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SystemVerilog –
Part 2: Universal Verification Methodology Language Reference Manual

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IEEE Std	FDIS	Report on voting
1800.2 (2017)	91/1713/FDIS	91/1725/RVD

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IEEE Std 1800.2™-2017

IEEE Standard for Universal Verification Methodology Language Reference Manual

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IEEE-SA Standards Board

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Accellera Systems Initiative—*The Universal Verification Methodology (UVM) pre-IEEE Class Reference*.

Abstract: The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.

Keywords: agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction level modeling, verification methodology

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Introduction

This introduction is not part of IEEE Std 1800.2-2017, IEEE Standard for Universal Verification Methodology Language Reference Manual.

Verification has evolved into a complex project that often spans internal and external teams, but the discontinuity associated with multiple, incompatible methodologies among those teams can limit productivity. The Universal Verification Methodology (UVM) Language Reference Manual (LRM) addresses verification complexity and interoperability within companies and throughout the electronics industry for both novice and advanced teams while also providing consistency. While UVM is revolutionary, being the first verification methodology to be standardized, it is also evolutionary, as it is built on the Open Verification Methodology (OVM), which combined the Advanced Verification Methodology (AVM) with the Universal Reuse Methodology (URM) and concepts from the ***e*** Reuse Methodology (eRM). Furthermore, UVM also infuses concepts and code from the Verification Methodology Manual (VMM), plus the collective experience and knowledge of the over 300 members of the Accellera UVM Working Group to help standardize verification methodology. Finally, the transaction level modeling (TLM) facilities in UVM are based on what was developed by Open SystemC Initiative (OSCI) for SystemC, though they are not an exact replication or re-implementation of the SystemC TLM library.

IEEE Standard for Universal Verification Methodology Language Reference Manual

1. Overview

1.1 Scope

This standard establishes the Universal Verification Methodology (UVM), a set of application programming interfaces (APIs) that defines a base class library (BCL) definition used to develop modular, scalable, and reusable components for functional verification environments. The APIs and BCL are based on the IEEE standard for SystemVerilog, IEEE Std 1800™.[1]

1.2 Purpose

Verification components and environments are currently created in different forms, making interoperability among verification tools and/or geographically dispersed design environments both time consuming to develop and error prone. The results of the UVM standardization effort will improve interoperability and reduce the cost of repurchasing and rewriting *intellectual property* (IP) for each new project or electronic design automation (EDA) tool, as well as make it easier to reuse verification components. Overall, the UVM standardization effort will lower verification costs and improve design quality throughout the industry.

1.3 Conventions used

The conventions used throughout the document are as follows:

— UVM is case-sensitive.

— Any syntax examples shown in this standard are informative. They are intended to illustrate the usage of UVM constructs in a simple context and do not define the full syntax.

1.3.1 Visual cues (meta-syntax)

Bold shows required keywords and/or special characters, e.g., **uvm_component**.

Italics shows variables or definitions, e.g., *name* or *Globals*.

`Courier` shows SystemVerilog examples, external command names, directories and files, etc., e.g., an implementation needs to call `super.do_copy`.

[1]Information on references can be found in Clause 2.

The asterisk (*) symbol, when combined with a prefix and/or postfix denoting a part of the construct, represents a series of construct names with exactly this prefix and/or postfix, e.g., `class uvm_*_port`.

1.3.2 Return values

a) Equivalent terms:
   1) "TRUE," "True," and "true" are equivalent to each other and used interchangeably throughout this document.
   2) "FALSE," "False," and "false" are equivalent to each other and used interchangeably throughout this document.
b) A bit value of `1` is treated as TRUE and `0` is treated as FALSE.
c) Conversely, TRUE refers to `1` and FALSE refers to `0` for return values.
d) Datatypes returned:
   1) For a bit or integer, `1` (or `1'b1`) or `0` (`1'b0`) is acceptable.
   2) For an enumerated type, TRUE or FALSE is acceptable.
e) For functions that return `TRUE/FALSE`, if only one returned value is defined (e.g., for `TRUE`), then the opposite return value shall be inferred (for all other possibilities).

1.3.3 Inheritance

Class declarations shown in this document may be of the form *class A* extends *B*. These declarations do not imply *class A* and *class B* are adjacent in the inheritance tree; implementations are free to have other classes between *A* and *B* in the inheritance tree, e.g.,

```
class X extends B;
      // body of class X
   endclass
class A extends X;
      // body of class A
   endclass
```

would comply.

The API and the semantics of the API from a base class shall be present in any derived classes, unless that API is overridden by an explicitly documented API within the derived class.

1.3.4 Operation order on equivalent data objects

The functionality described in this document typically operates on a set of data objects. An implementation and/or the underlying run-time engine may choose any operation order or sorting order for "equivalent data" objects within the specified semantics.

As a result of this policy, results returned and/or sequential behavior and/or produced output may differ between implementations and/or different underlying engines.

It is up to the user to establish an operation order if necessary.

1.3.5 uvm_pkg

All properties of UVM, including classes, global methods, and variables, are exported via the `uvm_pkg` package. They may be accessed via `import` or via the Scope Resolution operator (`::`).

UVM does not require any specific time unit precision for `uvm_pkg`.

All UVM methods that operate on values of type `time`, such as **uvm_printer::print_time** (see 16.2.3.11), are subject to the time scaling defined in IEEE Std 1800™.

1.3.6 Random stability

Any APIs that result in user code being executed are not guaranteed to be random stable. All other APIs are guaranteed to be random stable, unless otherwise specified.

2. Normative references

The following referenced documents are indispensable for the application of this standard (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1800™, IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language.[2, 3]

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