Guide for the standard probe pad sizes and layouts for wafer-level electrical testing

PUBLICLY AVAILABLE SPECIFICATION

IEC/PAS 62203
Edition 1.0
2000-11
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Published by

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Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201
INTERNATIONAL ELECTROTECHNICAL COMMISSION

GUIDE FOR THE STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER-LEVEL ELECTRICAL TESTING

FOREWORD

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public and established in an organization operating under given procedures.

IEC-PAS 62203 was submitted by JEDEC and has been processed by IEC technical committee 47: Semiconductor devices.

The text of this PAS is based on the following document:

Draft PAS

IEC-PAS 62203

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Report on voting

IEC-PAS 62203

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GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS
FOR WAFER-LEVEL ELECTRICAL TESTING

(From JEDEC Ballot JCB-96-27, formulated under the cognizance of JC14.2 Committee on Wafer-Level Reliability)

1 Scope

This guide applies to double- and single-column arrays of metal probe pads, on a semiconductor wafer or chip, that are electrically connected to one or more test structures.

The use of this guide will make necessary only two standard wafer-probe cards, one with a 1-by-16 and the other with a 2-by-16 standard array of probe tips to make contact with probe pads.

This guide is intended, in particular, to facilitate and expedite wafer-level electrical testing by laboratories participating in interlaboratory experiments conducted by JC-14.2 Committee.

This guide is intended, in general, to facilitate and expedite wafer-level electrical testing of test structures when using a wafer-probe card to make electrical contact to these structures.

The use of this guide will impose some restrictions on how test structures may be grouped within and near the area defined by the array of pads.