



IEC 60747-8

Edition 3.1 2021-06
CONSOLIDATED VERSION

INTERNATIONAL STANDARD



**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.080.30

ISBN 978-2-8322-9959-3

Warning! Make sure that you obtained this publication from an authorized distributor.



IEC 60747-8

Edition 3.1 2021-06
CONSOLIDATED VERSION

REDLINE VERSION



Semiconductor devices – Discrete devices – Part 8: Field-effect transistors

CONTENTS

FOREWORD	6
1 Scope	8
2 Normative references	8
3 Terms and definitions	9
3.1 Types of field-effect transistors	9
3.2 General terms	10
3.2.1 Physical regions (of a field-effect transistor)	10
3.2.2 Functional regions	11
3.3 Terms related to ratings and characteristics	12
3.4 Conventional used terms	17
4 Letter symbols	17
4.1 General	17
4.2 Additional general subscripts	17
4.3 List of letter symbols	17
4.3.1 Voltage	17
4.3.2 Currents	18
4.3.3 Power dissipation	19
4.3.4 Small-signal parameters	19
4.3.5 Other parameters	20
4.3.6 Matched-pair field-effect transistors	21
4.3.7 Inverse diodes integrated in MOSFETs for N-channel	21
5 Essential ratings and characteristics	22
5.1 General	22
5.1.1 Device categories	22
5.1.2 Multiple-gate devices	22
5.1.3 Handling precautions	22
5.2 Ratings (limiting values)	22
5.2.1 Temperatures	22
5.2.2 Power dissipation (P_{tot})	22
5.2.3 Safe operating area (SOA) for MOSFET only	22
5.2.4 Voltages and currents	23
5.3 Characteristics	24
5.3.1 Characteristics for low-frequency amplifier	24
5.3.2 Characteristics for high-frequency amplifier	25
5.3.3 Characteristics for high and low power switching and chopper	27
5.3.4 Characteristics for low-level amplifier	30
5.3.5 Characteristics for voltage-controlled resistor	32
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential	33
6 Measuring methods	34
6.1 General	34
6.2 Verification of ratings (limiting values)	34
6.2.1 Voltages and currents	34
6.2.2 Safe operating area	40
6.2.3 Avalanche energy	45

6.3	Methods of measurement	47
6.3.1	Breakdown voltage, drain to source ($V_{(BR)DS^*}$)	47
6.3.2	Gate-source off-state voltage ($V_{GS(off)}$) (type A and B), gate source threshold voltage ($V_{GS(th)}$) (type C)	48
6.3.3	Drain leakage current (d.c.) (I_{DS^*})(type C), Drain cut-off current (d.c.) (I_{DSX}) (type A and B)	49
6.3.4	Gate cut-off current (I_{GS^*})(type A), Gate-leakage current (I_{GS^*})(type B and C)	49
6.3.5	(Static) drain-source on-state resistance ($r_{DS(on)}$) or drain-source on-state voltage ($V_{DS(on)}$)	50
6.3.6	Switching times ($t_{d(on)}$, t_r , $t_{d(off)}$, and t_f)	52
6.3.7	Turn-on power dissipation (P_{on}), turn-on energy (per pulse) (E_{on})	53
6.3.8	Turn-off power dissipation (P_{off}), turn-off energy (per pulse) (E_{off})	54
6.3.9	Gate charges (Q_G , Q_{GD} , $Q_{GS(th)}$, $Q_{GS(pl)}$)	54
6.3.10	Common source short-circuit input capacitance (C_{iss})	55
6.3.11	Common source short-circuit output capacitance (C_{oss})	56
6.3.12	Common source short-circuit reverse transfer capacitance (C_{rss})	57
6.3.13	Internal gate resistance (r_g)	58
6.3.14	MOSFET forward recovery time (t_{fr}) and MOSFET forward recovered charge (Q_f)	59
6.3.15	Drain-source reverse voltage (V_{DSR} V_{SD})	64
6.3.16	Small-signal short-circuit output conductance (type A, B and C) (g_{oss})	64
6.3.17	Small-signal short-circuit forward transconductance (types A, B and C)	67
6.3.18	Noise (types A, B and C) (F , V_n)	69
6.3.19	On-state drain-source resistance (under small-signal conditions) ($r_{ds(on)}$)	70
6.3.20	Channel-case transient thermal impedance ($Z_{th(j-c)}$) and thermal resistance ($R_{th(j-c)}$) of a field-effect transistor	71
7	Acceptance and reliability	73
7.1	General requirements	73
7.2	Acceptance-defining characteristics	73
7.3	Endurance and reliability tests	74
7.3.1	High-temperature blocking (HTRB)	74
7.3.2	High-temperature gate bias	74
7.3.3	Intermittent operating life (load cycles)	74
7.4	Type tests and routine tests	75
7.4.1	Type tests	75
7.4.2	Routine tests	75
	Bibliography	77
	Figure 1 – Basic waveforms to specify the gate charges	14
	Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}	16
	Figure 3 – Switching times	21
	Figure 4 – Circuit diagram for testing of drain-source voltage	35
	Figure 5 – Circuit diagram for testing of gate-source voltage	35
	Figure 6 – Circuit diagram for testing of gate-drain voltage	36
	Figure 7 – Basic circuit for the testing of drain current	37

Figure 8 – Circuit diagram for testing of peak drain current	38
Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs	38
Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs	39
Figure 11 – Circuit diagram for verifying FBSOA	40
Figure 12 – Circuit diagram for verifying RBSOA	41
Figure 13 – Test waveforms for verifying RBSOA	42
Figure 14 – Circuit for testing safe operating pulse duration at load short circuit	43
Figure 15 – Waveforms of gate-source voltage V_{GS} , drain current I_D and voltage V_{DS} during load short circuit condition SCSOA	43
Figure 16 – Circuit for the inductive avalanche switching	45
Figure 17 – Waveforms of I_D , V_{DS} and V_{GS} during unclamped inductive switching	45
Figure 18 – Waveforms of I_D , V_{DS} and V_{GS} for the non-repetitive avalanche switching	46
Figure 19 – Circuit diagrams for the measurement drain-source breakdown voltage	47
Figure 20 – Circuit diagram for measurement of gate-source off-state voltage and gate- source threshold voltage	48
Figure 21 – Circuit diagram for drain leakage (or off-state) current or drain cut-off current measurement	49
Figure 22 – Circuit diagram for measuring of gate cut-off current or gate leakage current	50
Figure 23 – Basic circuit of measurement for on-state resistance	51
Figure 24 – On-state resistance	51
Figure 25 – Circuit diagram for switching time	52
Figure 26 – Schematic switching waveforms and times	52
Figure 27 – Circuit for determining the turn-on and turn-off power dissipation and/or energy	53
Figure 28 – Circuit diagrams for the measurement gate charges	55
Figure 29 – Basic for the measurement of short-circuit input capacitance	56
Figure 30 – Basic circuit for measurement of short-circuit output capacitance (C_{OSS})	57
Figure 31 – Circuit for measurement of reverse transfer capacitance C_{RSS}	58
Figure 32 – Circuit for measurement of internal gate resistance	59
Figure 33 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 1)	60
Figure 34 – Current waveform through MOSFET (Method 1)	61
Figure 35 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 2)	62
Figure 36 – Current waveform through MOSFET (Method 2)	63
Figure 37 – Circuit diagram for the measurement of drain-source reverse voltage	64
Figure 38 – Basic circuit for the measurement of the output conductance g_{OSS} (method 1: null method)	65
Figure 39 – Basic circuit for the measurement of the output conductance g_{OSS} (method 2: two-voltmeter method)	66
Figure 40 – Circuit for the measurement of short-circuit forward transconductance g_{fS} (Method 1: Null method)	67
Figure 41 – Circuit for the measurement of forward transconductance g_{fS} (method 2: two-voltmeter method)	68
Figure 42 – Block diagram for the measurement of equivalent input noise voltage	69

Figure 43 – Circuit for the measurement of equivalent input noise voltage	69
Figure 44 – Circuit diagram for the measurement of on-state drain-source resistance	70
Figure 45 – Circuit diagram	71
Figure 46 – Circuit for high-temperature blockings	74
Figure 47 – Circuit for high-temperature gate bias	74
Figure 48 – Circuit for intermittent operating life	75
Table 1 – Terms for MOSFET in this standard document and the conventional used terms for the inverse diode integrated in the MOSFETs for N-channel	17
Table 2 – Acceptance defining characteristics	34
Table 3 – Acceptance-defining characteristics for endurance and reliability tests	73
Table 4 – Minimum type and routine tests for FETs when applicable	76

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 8: Field-effect transistors

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.

IEC 60747-8 edition 3.1 contains the third edition (2010-12) [documents 47E/398/FDIS and 47E/406/RVD] and its amendment 1 (2021-06) [documents 47E/726/CDV and 47E/744/RVC].

In this Redline version, a vertical line in the margin shows where the technical content is modified by amendment 1. Additions are in green text, deletions are in strikethrough red text. A separate Final version with all changes accepted is available in this publication.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

- a) "Clause 3 Classification" was moved and added to Clause 1.
- b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
- c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

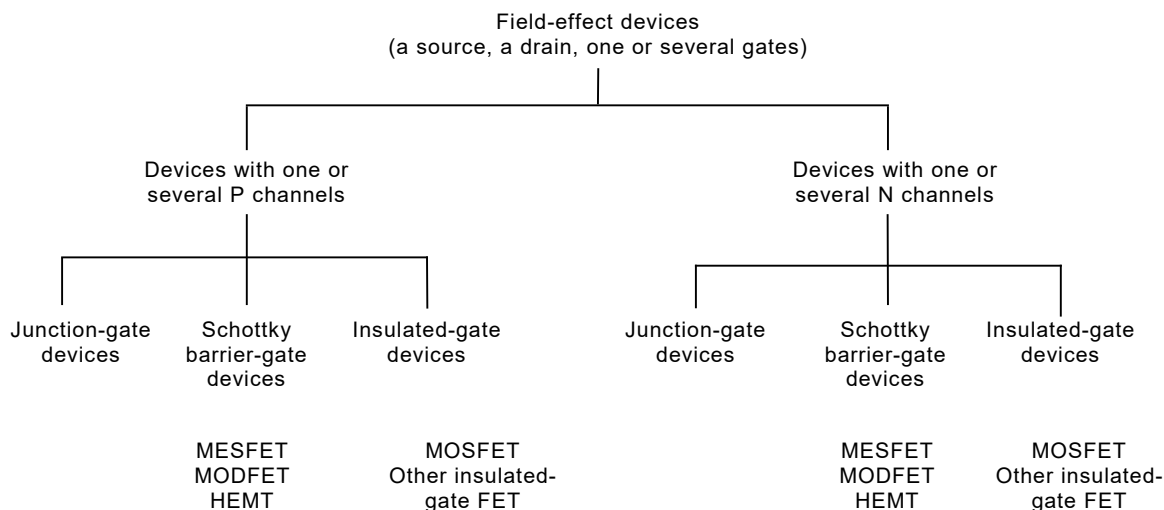
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion (normally on) type;
- type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-8:2010+AMD1:2021 CSV – 9 –

© IEC 2021

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*



IEC 60747-8

Edition 3.1 2021-06
CONSOLIDATED VERSION

FINAL VERSION

**Semiconductor devices – Discrete devices –
Part 8: Field-effect transistors**

CONTENTS

FOREWORD	6
1 Scope	8
2 Normative references	8
3 Terms and definitions	9
3.1 Types of field-effect transistors	9
3.2 General terms	10
3.2.1 Physical regions (of a field-effect transistor)	10
3.2.2 Functional regions	11
3.3 Terms related to ratings and characteristics	12
3.4 Conventional used terms	17
4 Letter symbols	17
4.1 General	17
4.2 Additional general subscripts	17
4.3 List of letter symbols	17
4.3.1 Voltage	17
4.3.2 Currents	18
4.3.3 Power dissipation	18
4.3.4 Small-signal parameters	18
4.3.5 Other parameters	20
4.3.6 Matched-pair field-effect transistors	21
4.3.7 Inverse diodes integrated in MOSFETs for N-channel	21
5 Essential ratings and characteristics	22
5.1 General	22
5.1.1 Device categories	22
5.1.2 Multiple-gate devices	22
5.1.3 Handling precautions	22
5.2 Ratings (limiting values)	22
5.2.1 Temperatures	22
5.2.2 Power dissipation (P_{tot})	22
5.2.3 Safe operating area (SOA) for MOSFET only	22
5.2.4 Voltages and currents	23
5.3 Characteristics	23
5.3.1 Characteristics for low-frequency amplifier	23
5.3.2 Characteristics for high-frequency amplifier	25
5.3.3 Characteristics for high and low power switching and chopper	27
5.3.4 Characteristics for low-level amplifier	30
5.3.5 Characteristics for voltage-controlled resistor	32
5.3.6 Specific characteristics of matched-pair field-effect transistors for low-frequency differential	33
6 Measuring methods	34
6.1 General	34
6.2 Verification of ratings (limiting values)	34
6.2.1 Voltages and currents	34
6.2.2 Safe operating area	40
6.2.3 Avalanche energy	44

6.3	Methods of measurement	46
6.3.1	Breakdown voltage, drain to source ($V_{(BR)DS^*}$)	46
6.3.2	Gate-source off-state voltage ($V_{GS(off)}$) (type A and B), gate source threshold voltage ($V_{GS(th)}$) (type C).....	47
6.3.3	Drain leakage current (d.c.) (I_{DS^*})(type C), Drain cut-off current (d.c.) (I_{DSX}) (type A and B).....	48
6.3.4	Gate cut-off current (I_{GS^*})(type A), Gate-leakage current (I_{GS^*})(type B and C).....	48
6.3.5	(Static) drain-source on-state resistance ($r_{DS(on)}$) or drain-source on-state voltage ($V_{DS(on)}$)	49
6.3.6	Switching times ($t_{d(on)}$, t_r , $t_{d(off)}$, and t_f)	51
6.3.7	Turn-on power dissipation (P_{on}), turn-on energy (per pulse) (E_{on})	52
6.3.8	Turn-off power dissipation (P_{off}), turn-off energy (per pulse) (E_{off}).....	53
6.3.9	Gate charges (Q_G , Q_{GD} , $Q_{GS(th)}$, $Q_{GS(pl)}$).....	53
6.3.10	Common source short-circuit input capacitance (C_{iss}).....	54
6.3.11	Common source short-circuit output capacitance (C_{oss})	55
6.3.12	Common source short-circuit reverse transfer capacitance (C_{rss}).....	56
6.3.13	Internal gate resistance (r_g).....	57
6.3.14	MOSFET forward recovery time (t_{fr}) and MOSFET forward recovered charge (Q_f).....	58
6.3.15	Drain-source reverse voltage (V_{SD})	62
6.3.16	Small-signal short-circuit output conductance (type A, B and C) (g_{oss})	62
6.3.17	Small-signal short-circuit forward transconductance (types A, B and C).....	65
6.3.18	Noise (types A, B and C) (F, V_n)	67
6.3.19	On-state drain-source resistance (under small-signal conditions) ($r_{ds(on)}$)	68
6.3.20	Channel-case transient thermal impedance ($Z_{th(j-c)}$) and thermal resistance ($R_{th(j-c)}$) of a field-effect transistor	69
7	Acceptance and reliability.....	71
7.1	General requirements.....	71
7.2	Acceptance-defining characteristics	71
7.3	Endurance and reliability tests.....	72
7.3.1	High-temperature blocking (HTRB)	72
7.3.2	High-temperature gate bias	72
7.3.3	Intermittent operating life (load cycles)	72
7.4	Type tests and routine tests	73
7.4.1	Type tests	73
7.4.2	Routine tests	73
	Bibliography.....	75
	Figure 1 – Basic waveforms to specify the gate charges	14
	Figure 2 – Integral times for the turn-on energy E_{on} and turn-off energy E_{off}	16
	Figure 3 – Switching times	21
	Figure 4 – Circuit diagram for testing of drain-source voltage.....	35
	Figure 5 – Circuit diagram for testing of gate-source voltage.....	35
	Figure 6 – Circuit diagram for testing of gate-drain voltage	36
	Figure 7 – Basic circuit for the testing of drain current	37

Figure 8 – Circuit diagram for testing of peak drain current	38
Figure 9 – Basic circuit for the testing of reverse drain current of MOSFETs	38
Figure 10 – Basic circuit for the testing of peak reverse drain current of MOSFETs	39
Figure 11 – Circuit diagram for verifying FBSOA	40
Figure 12 – Circuit diagram for verifying RBSOA	41
Figure 13 – Test waveforms for verifying RBSOA	41
Figure 14 – Circuit for testing safe operating pulse duration at load short circuit	42
Figure 15 – Waveforms of gate-source voltage V_{GS} , drain current I_D and voltage V_{DS} during load short circuit condition SCSOA	43
Figure 16 – Circuit for the inductive avalanche switching	44
Figure 17 – Waveforms of I_D , V_{DS} and V_{GS} during unclamped inductive switching	44
Figure 18 – Waveforms of I_D , V_{DS} and V_{GS} for the non-repetitive avalanche switching	45
Figure 19 – Circuit diagrams for the measurement drain-source breakdown voltage	46
Figure 20 – Circuit diagram for measurement of gate-source off-state voltage and gate- source threshold voltage	47
Figure 21 – Circuit diagram for drain leakage (or off-state) current or drain cut-off current measurement	48
Figure 22 – Circuit diagram for measuring of gate cut-off current or gate leakage current	49
Figure 23 – Basic circuit of measurement for on-state resistance	50
Figure 24 – On-state resistance	50
Figure 25 – Circuit diagram for switching time	51
Figure 26 – Schematic switching waveforms and times	51
Figure 27 – Circuit for determining the turn-on and turn-off power dissipation and/or energy	52
Figure 28 – Circuit diagrams for the measurement gate charges	54
Figure 29 – Basic for the measurement of short-circuit input capacitance	55
Figure 30 – Basic circuit for measurement of short-circuit output capacitance (C_{OSS})	56
Figure 31 – Circuit for measurement of reverse transfer capacitance C_{RSS}	57
Figure 32 – Circuit for measurement of internal gate resistance	58
Figure 33 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 1)	59
Figure 34 – Current waveform through MOSFET (Method 1)	59
Figure 35 – Circuit diagram for MOSFET forward recovery time and recovered charge (Method 2)	60
Figure 36 – Current waveform through MOSFET (Method 2)	61
Figure 37 – Circuit diagram for the measurement of drain-source reverse voltage	62
Figure 38 – Basic circuit for the measurement of the output conductance g_{OSS} (method 1: null method)	63
Figure 39 – Basic circuit for the measurement of the output conductance g_{OSS} (method 2: two-voltmeter method)	64
Figure 40 – Circuit for the measurement of short-circuit forward transconductance g_{fS} (Method 1: Null method)	65
Figure 41 – Circuit for the measurement of forward transconductance g_{fS} (method 2: two-voltmeter method)	66
Figure 42 – Block diagram for the measurement of equivalent input noise voltage	67

Figure 43 – Circuit for the measurement of equivalent input noise voltage	67
Figure 44 – Circuit diagram for the measurement of on-state drain-source resistance	68
Figure 45 – Circuit diagram	69
Figure 46 – Circuit for high-temperature blockings	72
Figure 47 – Circuit for high-temperature gate bias	72
Figure 48 – Circuit for intermittent operating life	73
Table 1 – Terms for MOSFET in this document and the conventional used terms for the inverse diode integrated in the MOSFETs for N-channel	17
Table 2 – Acceptance defining characteristics	34
Table 3 – Acceptance-defining characteristics for endurance and reliability tests	71
Table 4 – Minimum type and routine tests for FETs when applicable	74

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

Part 8: Field-effect transistors

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.

IEC 60747-8 edition 3.1 contains the third edition (2010-12) [documents 47E/398/FDIS and 47E/406/RVD] and its amendment 1 (2021-06) [documents 47E/726/CDV and 47E/744/RVC].

This Final version does not show where the technical content is modified by amendment 1. A separate Redline version with all changes highlighted is available in this publication.

International Standard IEC 60747-8 has been prepared by subcommittee 47E: Discrete semiconductor devices, of IEC technical committee 47: Semiconductor devices.

This third edition constitutes a technical revision.

The main changes with respect to the previous edition are listed below.

- a) "Clause 3 Classification" was moved and added to Clause 1.
- b) "Clause 4 Terminology and letter symbols" was divided into "Clause 3 Terms and definitions" and "Clause 4 Letter symbols" was amended with additions and deletions.
- c) Clause 5, 6 and 7 were amended with necessary additions and deletions.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

This Part 8 should be used in conjunction with IEC 60747-1:2006.

A list of all the parts in the IEC 60747 series, under the general title *Semiconductor devices – Discrete devices*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

The committee has decided that the contents of the base publication and its amendment will remain unchanged until the stability date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

SEMICONDUCTOR DEVICES – DISCRETE DEVICES –

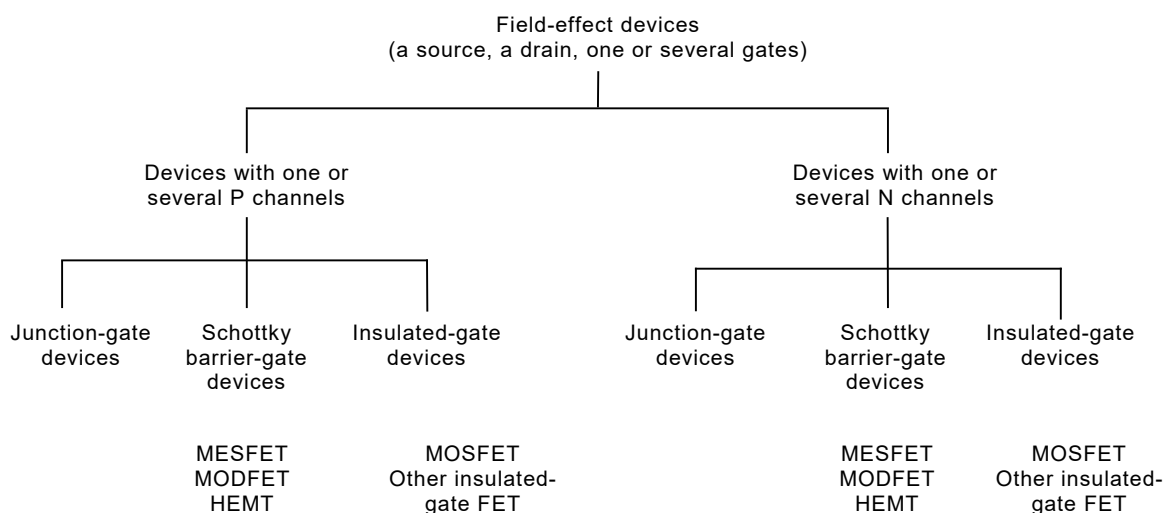
Part 8: Field-effect transistors

1 Scope

This part of IEC 60747 gives standards for the following categories of field-effect transistors:

- type A: junction-gate type;
- type B: insulated-gate depletion (normally on) type;
- type C: insulated-gate enhancement (normally off) type.

Since a field-effect transistor may have one or several gates, the classification shown below results:



NOTE 1 Schottky barrier-gate and insulated gate devices include depletion type devices and enhancement type devices.

NOTE 2 MOSFETs for some applications may not have inverse diode characteristics in the data sheet. Special circuit element structures to eliminate body diode are under development for such applications. MOSFET applications such as motor control equipment need to specify the inverse diode characteristics in the MOSFET to use the inverse diode as a free wheeling diode.

NOTE 3 The graphical symbol only for type C is used in this standard. The standard equally applies for P-channel and for type A and B devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61340 (all parts), *Electrostatics*

IEC 60747-1:2006, *Semiconductor devices – Part 1: General*

IEC 60747-8:2010+AMD1:2021 CSV

– 9 –

© IEC 2021

IEC 60747-7:2000, *Semiconductor devices – Part 7: Bipolar transistors*

IEC 60749-23:2004, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

IEC 60749-34, *Semiconductor devices – Mechanical and climatic test methods – Part 34: Power cycling*