TECHNICAL SPECIFICATION

IEC TS 62404

First edition
2007-02

Logic digital integrated circuits – Specification for I/O interface model for integrated circuit (IMIC version 1.3)

International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch

Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE XB

For price, see current catalogue

CONTENTS

FOREWORD 4
INTRODUCTION 6

1 Scope 7
2 Normative references 7
3 Terms and definitions 7
4 Outline 7
4.1 General 7
4.2 Covered range of model 8
4.3 Language for circuits 8
4.4 Device model 8
4.5 Structure of model 8
4.6 Simulation 8
4.7 Relation to IBIS 8
5 Model structure 9
6 Detailed model description 14
6.1 Description rules 14
6.2 IC model file 16
6.3 Package model file 42
6.4 Module model file 49
7 Levels of models 56

Annex A (informative) Model delivery flow 58
Annex B (informative) Example of model description 59

Figure 1 – Outline of the model 8
Figure 2 – Hierarchy of three models 9
Figure 3 – Data structure of an IMIC model file for IC 11
Figure 4 – Data structure of an IMIC model file for package 12
Figure 5 – Data structure of an IMIC model file for module 13
Figure 6 – Pad assignment 20
Figure 7 – Example of circuit description 24
Figure 8 – Input stimulus 25
Figure 9 – Diode equivalent circuit 29
Figure 10 – Diode characteristics 30
Figure 11 – NMOS transistor equivalent circuit 31
Figure 12 – PMOS transistor equivalent circuit 31
Figure 13 – Gate channel characteristics of MOS transistor 32
Figure 14 – Characteristics of diode in MOS transistor 33
Figure 15 – NPN transistor equivalent circuit 35
Figure 16 – PNP transistor equivalent circuit 35
Figure 17 – Static characteristics of bipolar transistor 35
Figure 18 – NMOS characteristics on regular grid 39

Figure 19 – MOS transistor model with two-terminal model 39
Figure 20 – Relationship between inner terminals and equivalent circuits of package 46
Figure 21 – Relationship between outer terminals and equivalent circuits of package 47
Figure 22 – Example of module circuit 53
Figure 23 – Example of signal source of module 55
Figure A.1 – Delivery flow of model files 58
Figure B.1 – IC structure 59
Figure B.2 – Equivalent circuit 59

Table 1 – Elements of model structures 10
Table 2 – Levels of models 57
Table 3 – Required elements of model for each level 57

INTERNATIONAL ELECTROTECHNICAL COMMISSION

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

The main task of IEC technical committees is to prepare International Standards. In exceptional circumstances, a technical committee may propose the publication of a technical specification when

- the required support cannot be obtained for the publication of an International Standard, despite repeated efforts, or
- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

IEC 62404, which is a technical specification, has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
47A/746/DTS	47A/751/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A bilingual version of this publication may be issued at a later date.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

With an increase in speed of electronic systems, it becomes necessary to accurately predict electrical performance including noise in electronic systems with integrated circuits.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of integrated circuits. Semiconductor manufacturers and/or suppliers are required by their users to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a non-disclosure agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for integrated circuits, which, approved as IEC 62014-1, has the following features:

- since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is drastically reduced;
- it is easy to get IBIS models that are supported by many simulation tools;
- a public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

- the modeling of power and ground currents is insufficient for accurate power and ground bounce analysis;
- since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry;
- in order to simulate EMI with accuracy, more information such as material constant and three-dimensional structures is needed.

LOGIC DIGITAL INTEGRATED CIRCUITS – SPECIFICATION FOR I/O INTERFACE MODEL FOR INTEGRATED CIRCUIT (IMIC version 1.3)

1 Scope

The following items are considered to standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electrical characteristics of equipment.

1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.
2) To define more flexible description rules for electric circuits in order to provide more accurate analysis of printed circuit board.
3) To introduce the concept of modeling levels to exchange relevant data for each application.
4) To enhance electrical modeling for packages and modules.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62014-1:2001, *Electronic design automation libraries – Part 1: Input/output buffer information specifications (IBIS version 3.2)*