

This is a preview - click here to buy the full publication



IEC 62527

Edition 1.0 2007-11

INTERNATIONAL STANDARD

IEEE 1450.2™

**Standard for extensions to Standard Test Interface Language (STIL) for d.c.
level specification**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE

W

ICS 25.040

ISBN 2-8318-9480-8

CONTENTS

FOREWORD.....	4
IEEE Introduction	7
1. Overview.....	8
1.1 Scope.....	9
1.2 Purpose.....	10
2. References.....	10
3. Definitions, acronyms, and abbreviations.....	10
3.1 Definitions	10
3.2 Acronyms and abbreviations	13
4. Structure of this standard	14
5. Extensions to Clause 6, STIL syntax description	14
5.1 Additional reserved words	14
5.2 DC expressions and units (dc_expr)	14
5.3 Additions to STIL name spaces and name resolution (IEEE Std 1450-1999, 6.16).....	15
6. Statement structure and organization of STIL information	15
6.1 Top-level statements and required ordering	15
6.2 Optional top-level statements	16
7. Extensions to Clause 8, STIL statement	16
7.1 STIL syntax.....	17
7.2 STIL example	17
8. Extensions to Clause 19, Spec and Selector blocks.....	17
9. Extensions to Clause 16, PatternExec block.....	17
9.1 PatternExec block syntax.....	17
9.2 PatternExec block example.....	18
9.3 DCLevels and DCSets usage in PatternExec and Pattern blocks	18
10. DCLevels block	18
10.1 DCLevels block syntax.....	19
10.2 DCLevels block example.....	31
10.3 InheritDCLevels Processing	33
10.4 InheritDCLevels example	33
11. DCSets block	34
11.1 DCSets block syntax.....	34
11.2 DCSets statement example	34

12.	DCSequence block	24
	12.1 DCSequence block syntax	25
	12.2 DCSequence example	26
13.	Extensions to Clause 18, WaveformTable block.....	28
	13.1 Event definition in WaveformTable block	28
	13.2 Mapping of event integers to DCLevels statements	29
	13.3 DC levels switching example	30
14.	Extensions to Clause 22, STIL Pattern statements	31
	14.1 DCLevels statement.....	31
	14.2 DCLevels statement example	31
	Annex A (informative) DCLevels and DCSets usage example.....	32
	Annex B (informative) Bibliography.....	38
	Annex C (informative) List of participantss.....	39

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**STANDARD FOR EXTENSIONS TO
STANDARD TEST INTERFACE LANGUAGE (STIL)
FOR DC LEVEL SPECIFICATION**

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
- 6) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC/IEEE 62527 has been processed through Technical Committee 93: Design automation.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1450.2(2005)	93/249/FDIS	93/260/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IEC/IEEE Dual Logo International Standards

This Dual Logo International Standard is the result of an agreement between the IEC and the Institute of Electrical and Electronics Engineers, Inc. (IEEE). The original IEEE Standard was submitted to the IEC for consideration under the agreement, and the resulting IEC/IEEE Dual Logo International Standard has been published in accordance with the ISO/IEC Directives.

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards.

Use of an IEC/IEEE Dual Logo International Standard is wholly voluntary. The IEC and IEEE disclaim liability for any personal injury, property or other damage, of any nature whatsoever, whether special, indirect, consequential, or compensatory, directly or indirectly resulting from the publication, use of, or reliance upon this, or any other IEC or IEEE Standard document.

The IEC and IEEE do not warrant or represent the accuracy or content of the material contained herein, and expressly disclaim any express or implied warranty, including any implied warranty of merchantability or fitness for a specific purpose, or that the use of the material contained herein is free from patent infringement. IEC/IEEE Dual Logo International Standards documents are supplied "AS IS".

The existence of an IEC/IEEE Dual Logo International Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEC/IEEE Dual Logo International Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

In publishing and making this document available, the IEC and IEEE are not suggesting or rendering professional or other services for, or on behalf of, any person or entity. Neither the IEC nor IEEE is undertaking to perform any duty owed by any other person or entity to another. Any person utilizing this, and any other IEC/IEEE Dual Logo International Standards or IEEE Standards document, should rely upon the advice of a competent professional in determining the exercise of reasonable care in any given circumstances.

Interpretations – Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments for revision of IEC/IEEE Dual Logo International Standards are welcome from any interested party, regardless of membership affiliation with the IEC or IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE-SA Standards Board, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA and/or General Secretary, IEC, 3, rue de Varembe, PO Box 131, 1211 Geneva 20, Switzerland.

Authorization to photocopy portions of any individual standard for internal or personal use is granted by the Institute of Electrical and Electronics Engineers, Inc., provided that the appropriate fee is paid to Copyright Clearance Center. To arrange for payment of licensing fee, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

NOTE – Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

**IEEE Standard for Extensions to
Standard Test Interface Language
(STIL) (IEEE Std 1450TM-1999)
for DC Level Specification**

Sponsor

Test Technology Standards Committee
of the
IEEE Computer Society

Approved 11 December 2002

IEEE-SA Standards Board

Abstract: This standard extends IEEE Std 1450-1999 (STIL) to support the definition of DC levels. STIL language constructs are defined to specify the DC conditions necessary to execute digital vectors on automated test equipment (ATE). STIL language extensions include structures for: (a) specifying the DC conditions for a device under test; (b) specifying DC conditions either globally, by pattern burst, by pattern, or by vector; (c) specifying alternate DC levels; and (d) selecting DC levels and alternate levels within a period, much the same as timed format events.

Keywords: automated test equipment (ATE), comparator, DC levels, device power supply (DPS), device under test (DUT), driver, driver termination, dynamic load, functional test, parametric measurement unit (PMU), power sequence, slew rate, voltage clamp

IEEE Introduction

Standard Test Interface Language (STIL) (IEEE Std 1450-1999) was developed and approved with an intentionally constrained scope. While DC levels were explicitly excluded from that scope, it was apparent that DC levels were an area of interest and importance to the STIL user community. The P1450.2 Working Group was formed to address the extension of DC levels to the STIL standard.

Three main topics were identified as priorities for the work. These include per-pin reference levels for signal pins (e.g., VIH, VIL, VOH, VOL), device power supply levels (voltage and current), and power sequencing to the device under test. During the course of development, two other important topics were addressed. These included the capability for switching levels within a period, and for switching levels between vectors in a pattern.

STANDARD FOR EXTENSIONS TO STANDARD TEST INTERFACE LANGUAGE (STIL) (IEEE Std 1450TM-1999) FOR DC LEVEL SPECIFICATION

1. Overview

This standard extends IEEE Std 1450-1999¹ (STIL) to support the definition of DC levels. The DC levels information consists of the per-pin reference levels, the device power supply (DPS) levels, and the sequencing of these levels for powering up the device, powering down the device, or changing levels of the device. The DC level definitions may be defined as static states that are established prior to execution of a pattern. They also may be selected within a pattern.

Figure 1 is a model of the test environment for a device under test (DUT) on an automatic test equipment (ATE) tester. Figure 2 is a model of the per-pin DC resources of an ATE tester. Figure 3 is a model of the differential DC resources of an ATE tester. The statements and blocks defined in this standard are defined relative to these models. Some functions represented by these models may not be available on some ATE systems. The DCSequence commands Apply and Connect load values into the hardware registers, e.g., VIL and VIH, and connect the tester resource, e.g., the driver, to the DUT, respectively.

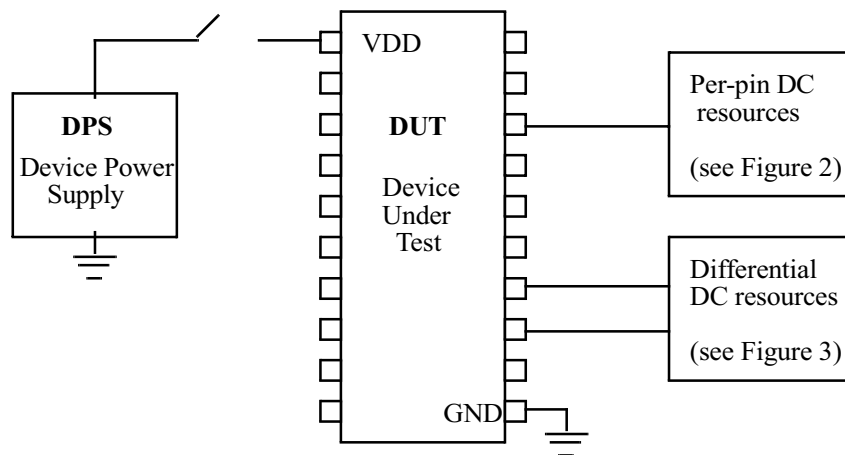


Figure 1—STIL model of DUT test environment on ATE tester

¹Information on references can be found in Clause 2.

1.1 Scope

This standard defines the following:

- a) Defines structures in STIL for specifying the DC conditions for a DUT. Examples of the DC conditions for device power supplies are DPS setup, power sequencing to the device, and power supply limiting/clamping. Examples of the DC conditions for commonly used signal references are VIL, VIH, VOL, VOH, IOL, IOH, VREF, VClampLow, and VClampHi.
- b) Defines structures in STIL such that the DC conditions may be specified either globally, by pattern burst, by pattern, or by vector.
- c) Defines structures in STIL to allow specification of alternate DC levels. Examples of commonly used alternate levels are VIHH, VIPP, and VILL.
- d) Defines structures in STIL such that the DC levels and alternate levels can be selected within a period, much the same as timed format events.

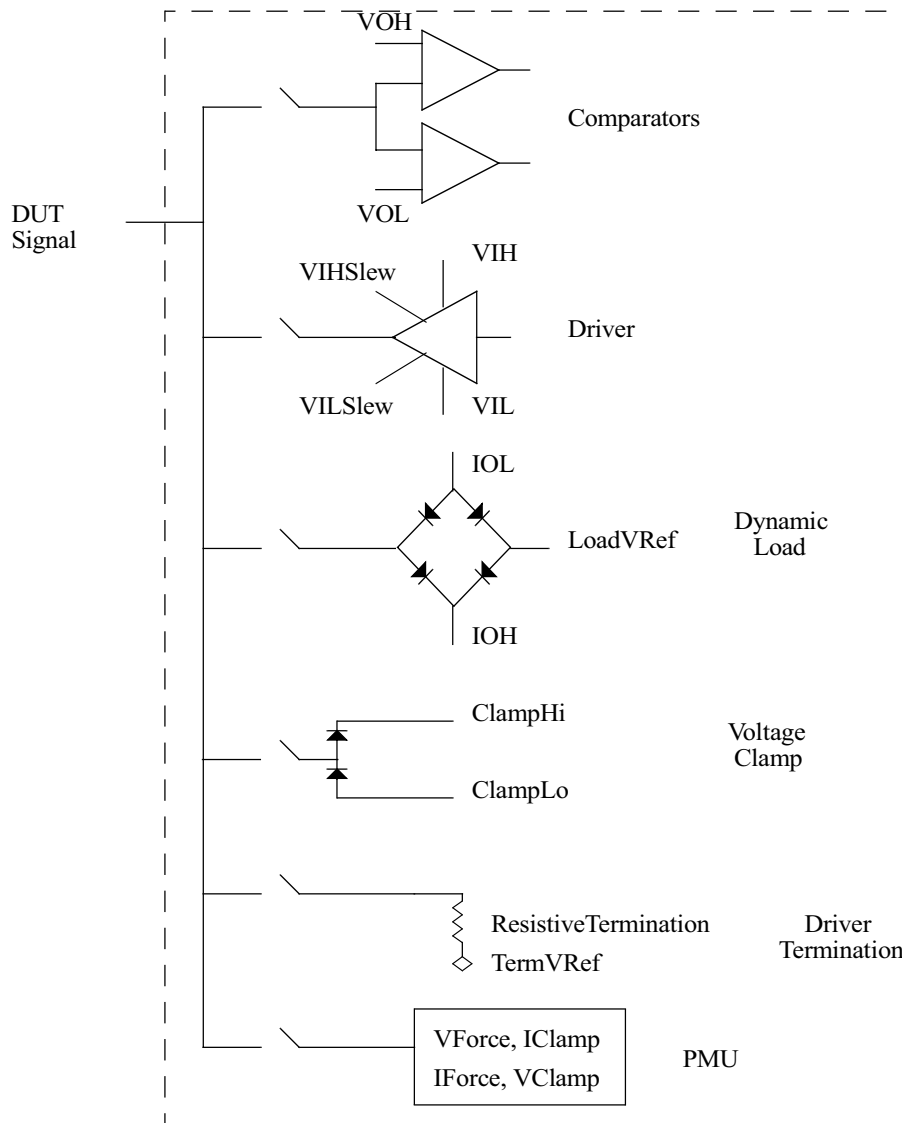


Figure 2—STIL model of per-pin DC resources of ATE tester

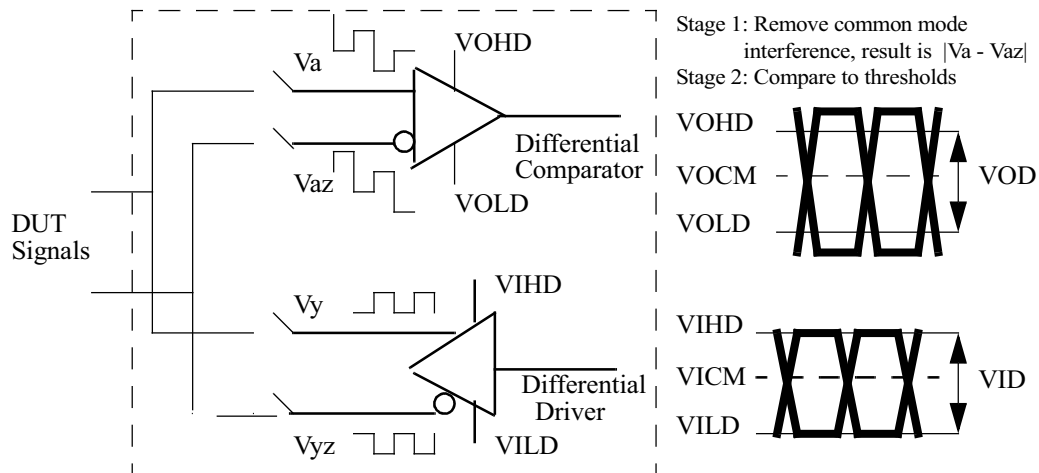


Figure 3—STIL model of differential DC resources of ATE tester

1.2 Purpose

This effort will define constructs in STIL to specify the DC conditions necessary to execute the digital vectors on ATE. This will complement the IEEE Std 1450-1999 definition, which defines structures for specification of timing and format information but does not define the DC conditions under which this information should be applied.

2. References

This standard shall be used in conjunction with the following standard. If the following standard is superseded by an approved revision, the revision shall apply.

IEEE Std 1450-1999, IEEE Standard Test Interface Language (STIL) for Digital Test Vectors.^{2, 3}

²The IEEE standards referred to in Clause 2 are trademarks owned by the Institute of Electrical and Electronics Engineers, Inc.

³IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (<http://standards.ieee.org/>).