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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1500(2005)	93/250/FDIS	93/261/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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IEEE Standard Testability Method for Embedded Core-based Integrated Circuits

Sponsor

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Approved 20 March 2005

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Abstract: This standard defines a mechanism for the test of core designs within a system on chip (SoC). This mechanism constitutes a hardware architecture and leverages the core test language (CTL) to facilitate communication between core designers and core integrators.
Keywords: core test, embedded core test, IP test, test reuse

IEEE Introduction

IEEE Std 1500 is a scalable standard architecture for enabling test reuse and integration for embedded cores and associated circuitry. It foregoes addressing analog circuits and focuses on facilitating efficient test of digital aspects of systems on chip (SoCs). IEEE Std 1500 has serial and parallel test access mechanisms (TAMs) and a rich set of instructions suitable for testing cores, SoC interconnect, and circuitry. In addition, IEEE Std 1500 defines features that enable core isolation and protection. IEEE Std 1500 will reduce test cost through improved automation, promote good design-for-test (DFT) technique, and improve test quality through improved access.

Core test language (CTL) is the official mechanism for describing IEEE 1500 wrappers and test data associated with cores. CTL is defined in IEEE P1450.6 ™[a] and was originally begun as part of the development of IEEE Std 1500.

IEEE Std 1500 was broadly influenced by the past work of the IEEE Std 1149.1™ Working Group and has several members from that group. IEEE Std 1149.1 and IEEE Std 1500 have similar goals at different levels of integration. IEEE Std 1149.1 describes a wrapper architecture and access mechanism designed for the purpose of testing components of a board whereas IEEE Std 1500 has a similar structure targeted towards testing cores in an SoC.

IEEE Std 1500 has been a continuous effort for its participants due to the goal of resolving the needs of reconciling and accommodating disparate test strategies and motives. The greatest effort has been put into supporting as many requirements as possible while still producing a cohesive and consistent standard.

Objective of the IEEE 1500 effort

The Embedded Core Test Working Group was approved in 1997 with the charter to develop a standard test method for integrated circuits (ICs) containing embedded cores, i.e., reusable megacells. That method would be independent of the underlying functionality of the IC or its individual embedded cores. The method will create the necessary testability requirements for detection and diagnosis of such ICs, while allowing for ease of interoperability of cores originated from distinct sources. This method will be usable for all classes of digital cores including hierarchical ones (subclause 15.1 discusses hierarchical core-wrapper configurations).

In order to satisfy that charter, the Embedded Core Test Working Group was organized into several task forces:

Core Test Language

Scalable Architecture

Compliance Definition/Information Model

Terminology/Glossary

Edition

Mergeable Cores Test

Benchmarking

Industry & Media Relations

[a]Information on references can be found in Clause 2.

Achievements

Since its inception, the Embedded Core Test Working Group has produced eight drafts of the preliminary standard, considering all aspects of core-based test. Due concern has been given to ensuring that a broad spectrum of users will be satisfied through flexibility. Both serial and parallel TAMs were developed. A definition for core wrappers was created, and a set of instructions developed. The CTL was begun, and an information model and compliance definition using that language were developed.

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STANDARD TESTABILITY METHOD FOR EMBEDDED CORE-BASED INTEGRATED CIRCUITS

1. Overview

IEEE Std 1500™ defines a scalable architecture for independent, modular test development and test application for embedded design blocks and also enables test of the external logic surrounding these cores. Modular testing is typically a requirement for embedded nonlogic blocks, such as memories, and for embedded predesigned nonmergeable intellectual property (IP) cores. In addition, the IEEE 1500 architecture can also be used to partition large design blocks into smaller blocks of more manageable size and to facilitate test reuse for blocks that are reused from one system-on-chip (SoC) design to the next.

The IEEE 1500 architecture comprises hardware requirements, through the definition of a standardized core wrapper, and uses a test-specific language to communicate information between core providers and core users. This language is the IEEE P1450.6™ [1] core test language (CTL). Although IEEE Std 1500 limited itself to test aspects internal to nonmergeable cores, careful consideration was given to the interoperability of such cores, resulting in plug-and-play (PnP) requirement definitions. SoC-specific issues such as those related to the design of test access mechanisms (TAMs) are excluded from this standard and assumed to be addressed by the SoC designer.

IEEE Std 1500 specifically focuses on defining test requirements for unidirectional non-tristate digital terminals, as these represent a minimum and mandatory set of requirements upon which the more complex bidirectional terminals are based. It is, therefore, implied that support for bidirectional or tristatable terminals is provided only to the extent that the individual unidirectional terminals, i.e., the bidirectional or tristatable terminal, are available for IEEE 1500 wrapper insertion. In addition, the hardware architecture defined in this standard anticipates a synchronous wrapper design methodology.

While IEEE Std 1500 does not discuss chip-level design, the architecture defined in this standard does not prevent interfacing with IEEE 1149.1™-based standards. An example of this interface is provided in Annex C for the reader's benefit.

All rules described in this standard apply to the case where the IEEE 1500 wrapper is enabled (the wrapper logic actively participates in the test of the core) except rules specific to the Wrapper Disabled state of the IEEE 1500 wrapper. In Wrapper Disabled state, the IEEE 1500 wrapper is disabled, allowing functional

[1] Information on references can be found in Clause 2.

operation of the wrapped core. IEEE P1450.6 constructs were added to this standard, where appropriate, to further guide the reader. It is anticipated that the reader will refer to these CTL constructs documented in IEEE P1450.6. Additional discussion that complements the body of this standard are presented in annex clauses:

— Annex A contains the legend for IEEE 1500 wrapper cells.

— Annex B shows examples of IEEE 1500 wrapper cells.

— Annex C presents similarities between IEEE Std 1500 and IEEE Std 1149.1 and discusses an example interface between IEEE Std 1500 and IEEE Std 1149.1.

1.1 Scope

IEEE Std 1500 has developed a standard design-for-testability method for integrated circuits (ICs) containing embedded nonmergeable cores. This method is independent of the underlying functionality of the IC or its individual embedded cores. The method creates the necessary requirements for the test of such ICs, while allowing for ease of interoperability of cores that may have originated from different sources.

1.2 Purpose

The aim of IEEE Std 1500 is to provide a consistent scalable solution to the test reuse challenges specific to the reuse of nonmergeable cores, while preserving the IP aspects that are often associated with these cores. This objective is achieved through provision of a core-centric methodology that enables successful integration of cores into SoCs.

IEEE Std 1500 provides a bridge between core providers and core users and also facilitates the automation of test data transfer and reuse between these two entities via the use of the IEEE P1450.6 CTL. This automation relies on information requirements (the information model) placed on the core provider to ensure that the core can be successfully integrated by the core user. The result is shorter time to market for core providers and core users.

The data transfer and reuse from the core provider to the core user are based on the premise that the core test data are left unchanged, while the test protocol is adapted from the IEEE 1500 hardware interface to the SoC.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture.[2]

IEEE P1450.6, Draft Standard for Standard Test Interface Language (STIL) for Digital Test Vector Data—Core Test Language (CTL), http://grouper.ieee.org/groups/ctl/.

[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA (http://standards.ieee.org/).