



IEC 62680-1-2

Edition 6.0 2022-09

# INTERNATIONAL STANDARD

## NORME INTERNATIONALE



**Universal serial bus interfaces for data and power –  
Part 1-2: Common components – USB Power Delivery specification**

**Interfaces de bus universel en série pour les données et l'alimentation  
électrique –  
Partie 1-2: Composants communs – Spécification de l'alimentation électrique  
par port USB**

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

COMMISSION  
ELECTROTECHNIQUE  
INTERNATIONALE

ICS 29.220; 33.120; 35.200

ISBN 978-2-8322-5288-8

**Warning! Make sure that you obtained this publication from an authorized distributor.  
Attention! Veuillez vous assurer que vous avez obtenu cette publication via un distributeur agréé.**

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

### UNIVERSAL SERIAL BUS INTERFACES FOR DATA AND POWER –

### Part 1-2: Common components – USB Power Delivery specification

#### FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62680-1-2 has been prepared by technical area 18: Multimedia home systems and applications for end-user networks, of IEC technical committee 100: Audio, video and multimedia systems and equipment.

The text of this standard was prepared by the USB Implementers Forum (USB-IF). The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

The text of this International Standard is based on the following documents:

Draft	Report on voting
100/3716/CDV	100/3763/RVC

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

A list of all parts in the IEC 62680 series, published under the general title *Universal serial bus interfaces for data and power*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under [webstore.iec.ch](http://webstore.iec.ch) in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

**IMPORTANT – The "colour inside" logo on the cover page of this document indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.**

## INTRODUCTION

The IEC 62680 series is based on a series of specifications that were originally developed by the USB Implementers Forum (USB-IF). These specifications were submitted to the IEC under the auspices of a special agreement between the IEC and the USB-IF.

This standard is the USB-IF publication Universal Serial Bus Power Delivery Specification Revision 3.1, Version 1.1.

The USB Implementers Forum, Inc.(USB-IF) is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. The Forum facilitates the development of high-quality compatible USB peripherals (devices), and promotes the benefits of USB and the quality of products that have passed compliance testing.

**ANY USB SPECIFICATIONS ARE PROVIDED TO YOU "AS IS," WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE USB IMPLEMENTERS FORUM AND THE AUTHORS OF ANY USB SPECIFICATIONS DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OR INFORMATION IN THIS SPECIFICATION.**

**THE PROVISION OF ANY USB SPECIFICATIONS TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.**

Entering into USB Adopters Agreements may, however, allow a signing company to participate in a reciprocal, RAND-Z licensing arrangement for compliant products. For more information, please see:

<https://www.usb.org/documents>

IEC DOES NOT TAKE ANY POSITION AS TO WHETHER IT IS ADVISABLE FOR YOU TO ENTER INTO ANY USB ADOPTERS AGREEMENTS OR TO PARTICIPATE IN THE USB IMPLEMENTERS FORUM."

**Universal Serial Bus  
Power Delivery Specification**

***Revision: 3.1***

***Version: 1.1***

***Release date: July 2021***

## LIMITED COPYRIGHT LICENSE

THE USB 3.0 PROMOTERS GRANT A CONDITIONAL COPYRIGHT LICENSE UNDER THE COPYRIGHTS EMBODIED IN THE USB POWER DELIVERY SPECIFICATION TO USE AND REPRODUCE THE SPECIFICATION FOR THE SOLE PURPOSE OF, AND SOLELY TO THE EXTENT NECESSARY FOR, EVALUATING WHETHER TO IMPLEMENT THE SPECIFICATION IN PRODUCTS THAT WOULD COMPLY WITH THE SPECIFICATION. WITHOUT LIMITING THE FOREGOING, USE THE OF SPECIFICATION FOR THE PURPOSE OF FILING OR MODIFYING ANY PATENT APPLICATION TO TARGET THE SPECIFICATION OR USB COMPLIANT PRODUCTS IS NOT AUTHORIZED. EXCEPT FOR THIS EXPRESS COPYRIGHT LICENSE, NO OTHER RIGHTS OR LICENSES ARE GRANTED, INCLUDING WITHOUT LIMITATION ANY PATENT LICENSES. IN ORDER TO OBTAIN ANY ADDITIONAL INTELLECTUAL PROPERTY LICENSES OR LICENSING COMMITMENTS ASSOCIATED WITH THE SPECIFICATION A PARTY MUST EXECUTE THE USB 3.0 ADOPTERS AGREEMENT. NOTE: BY USING THE SPECIFICATION, YOU ACCEPT THESE LICENSE TERMS ON YOUR OWN BEHALF AND, IN THE CASE WHERE YOU ARE DOING THIS AS AN EMPLOYEE, ON BEHALF OF YOUR EMPLOYER.

## INTELLECTUAL PROPERTY DISCLAIMER

THIS SPECIFICATION IS PROVIDED TO YOU “AS IS” WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE. THE AUTHORS OF THIS SPECIFICATION DISCLAIM ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS, RELATING TO USE OR IMPLEMENTATION OF INFORMATION IN THIS SPECIFICATION. THE PROVISION OF THIS SPECIFICATION TO YOU DOES NOT PROVIDE YOU WITH ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS.

Please send comments via electronic mail to [techsup@usb.org](mailto:techsup@usb.org)

For industry information, refer to the USB Implementers Forum web page at <http://www.usb.org>

USB Type-C® and USB4™ are trademarks of the Universal Serial Bus Implementers Forum (USB-IF). Thunderbolt™ is a trademark of Intel Corporation.

You may only use the Thunderbolt™ trademark or logo in conjunction with products designed to this specification that complete proper certification and executing a Thunderbolt™ trademark license – see <http://usb.org/compliance> for further information.

All product names are trademarks, registered trademarks, or service marks of their respective owners. Copyright © 2010-2021, USB 3.0 Promoter Group: Apple Inc., Hewlett-Packard Inc., Intel Corporation, Microsoft Corporation, Renesas, STMicroelectronics, and Texas Instruments.

All rights reserved.

## **Chairs**

Alvin Cox

Bob Dunstan

Deric Waters

Ed Berrios

Rahman Ismail

Richard Petrie

Cabling Sub-Chair

Specification Chair/Protocol Subgroup Chair

PHY Chair

Power Supply Chair

System Policy Chair

Specification Chair/Device Policy Chair

## **Editors**

Bob Dunstan

Richard Petrie

## **Contributors**

Charles Wang	ACON, Advanced-Connectek, Inc.	Sean O'Neal	Bizlink Technology, Inc.
Conrad Choy	ACON, Advanced-Connectek, Inc.	Tiffany Hsiao	Bizlink Technology, Inc.
Dennis Chuang	ACON, Advanced-Connectek, Inc.	Weichung Ooi	Bizlink Technology, Inc.
Steve Sedio	ACON, Advanced-Connectek, Inc.	Rahul Bhushan	Broadcom Corp.
Sunney Yang	ACON, Advanced-Connectek, Inc.	Asila nahas	Cadence Design Systems, Inc.
Vicky Chuang	ACON, Advanced-Connectek, Inc.	Claire Ying	Cadence Design Systems, Inc.
Joseph Scanlon	Advanced Micro Devices	Jie min	Cadence Design Systems, Inc.
Sujan Thomas	Advanced Micro Devices	Mark Summers	Cadence Design Systems, Inc.
Caspar Lin	Allion Labs, Inc.	Michal Staworko	Cadence Design Systems, Inc.
Casper Lee	Allion Labs, Inc.	Sathish Kumar	Cadence Design Systems, Inc.
Danny Shih	Allion Labs, Inc.	Ganesan	
Howard Chang	Allion Labs, Inc.	Alessandro	Canova Tech
Greg Stewart	Analogix Semiconductor, Inc.	Ingrassia	
Mehran Badii	Analogix Semiconductor, Inc.	Andrea Colognese	Canova Tech
Alexei Kosut	Apple	Antonio Orzelli	Canova Tech
Bill Cornelius	Apple	Davide Ghedin	Canova Tech
Carlos Colderon	Apple	Matteo Casalin	Canova Tech
Chris Uiterwijk	Apple	Michael Marioli	Canova Tech
Colin Whitby-Strevens	Apple	Nicola	Canova Tech
Corey Axelowitz	Apple	Scantamburlo	
Corey Lange	Apple	Paolo Pilla	Canova Tech
Dave Conroy	Apple	Yi-Feng Lin	Canyon Semiconductor
David Sekowski	Apple	YuHung Lin	Canyon Semiconductor
Girault Jones	Apple	David Tsai	Chrontel, Inc.
James Orr	Apple	Anshul Gulati	Cypress Semiconductor
Jason Chung	Apple	Anup Nayak	Cypress Semiconductor
Jay Kim	Apple	Benjamin Kropf	Cypress Semiconductor
Jeff Wilcox	Apple	Dhanraj Rajput	Cypress Semiconductor
Jennifer Tsai	Apple	Ganesh	Cypress Semiconductor
Karl Bowers	Apple	Subramaniam	
Keith Porthouse	Apple	Jagadeesan Raj	Cypress Semiconductor
Kevin Hsiue	Apple	Junjie cui	Cypress Semiconductor
Matt Mora	Apple	Manu Kumar	Cypress Semiconductor
Paul Baker	Apple	Muthu M	Cypress Semiconductor
Reese Schreiber	Apple	Nicholas Bodnaruk	Cypress Semiconductor
Ricardo Janezic	Apple	Pradeep Bajpai	Cypress Semiconductor
Pregitzer	Apple	Rajaram R	Cypress Semiconductor
Ruchi Chaturvedi	Apple	Rama Vakkantula	Cypress Semiconductor
Sameer Kelkar	Apple	Rushil Kadakia	Cypress Semiconductor
Sasha Tietz	Apple	Simon Nguyen	Cypress Semiconductor
Scott Jackson	Apple	Steven Wong	Cypress Semiconductor
Sree Raman	Apple	Subu Sankaran	Cypress Semiconductor
William Ferry	Apple	Sumeet Gupta	Cypress Semiconductor
Zaki Moussaoui	Apple	Tejender Sheoran	Cypress Semiconductor
Jeff Liu	ASMedia Technology Inc.	Venkat	Cypress Semiconductor
Kuo Lung Li	ASMedia Technology Inc.	Mandagulathar	
Ming-Wei Hsu	ASMedia Technology Inc.	Xiaofeng Shen	Cypress Semiconductor
PS Tseng	ASMedia Technology Inc.	Zeng Wei	Cypress Semiconductor
Sam Tzeng	ASMedia Technology Inc.	Adie Tan	Dell Inc.
Thomas Hsu	ASMedia Technology Inc.	Adolfo Montero	Dell Inc.
Weikao Chang	ASMedia Technology Inc.	Bruce Montag	Dell Inc.
Yang Cheng	ASMedia Technology Inc.	Gary Verdun	Dell Inc.
Shawn Meng	Bizlink Technology Inc.	Ken Nicholas	Dell Inc.
Bernard Shyu	Bizlink Technology, Inc.	Marcin Nowak	Dell Inc.
Eric Wu	Bizlink Technology, Inc.	Merle Wood	Dell Inc.
Morphy Hsieh	Bizlink Technology, Inc.	Mohammed Hijazi	Dell Inc.
		Siddhartha Reddy	Dell Inc.



Terry Matula	Dell Inc.	Fred Fons	Foxconn / Hon Hai
Jay Hu	Derun Semiconductor	Jie Zheng	Foxconn / Hon Hai
Shelly Liu	Derun Semiconductor	Patrick Casher	Foxconn / Hon Hai
Bindhu Vasu	Dialog Semiconductor (UK) Ltd	Steve Sedio	Foxconn / Hon Hai
Chanchal Gupta	Dialog Semiconductor (UK) Ltd	Terry Little	Foxconn / Hon Hai
Dipti Baheti	Dialog Semiconductor (UK) Ltd	Bob McVay	Fresco Logic Inc.
Duc Doan	Dialog Semiconductor (UK) Ltd	Christopher Meyers	Fresco Logic Inc.
Holger Petersen	Dialog Semiconductor (UK) Ltd	Dian Kurniawan	Fresco Logic Inc.
Jianming Yao	Dialog Semiconductor (UK) Ltd	Tom Burton	Fresco Logic Inc.
John Shi	Dialog Semiconductor (UK) Ltd	Abraham Levkoy	Google Inc.
KE Hong	Dialog Semiconductor (UK) Ltd	Adam Rodriguez	Google Inc.
Kevin Mori	Dialog Semiconductor (UK) Ltd	Alec Berg	Google Inc.
Larry Ping	Dialog Semiconductor (UK) Ltd	Benson Leung	Google Inc.
Mengfei Liu	Dialog Semiconductor (UK) Ltd	Chao Fei	Google Inc.
Scott Brown	Dialog Semiconductor (UK) Ltd	Dave Bernard	Google Inc.
Yimin Chen	Dialog Semiconductor (UK) Ltd	David Schneider	Google Inc.
Yong Li	Dialog Semiconductor (UK) Ltd	Diana Zigterman	Google Inc.
Justin Lee	Diodes Incorporated	Eric Herrmann	Google Inc.
Dan Ellis	DisplayLink (UK) Ltd.	Jim Guerin	Google Inc.
Jason Young	DisplayLink (UK) Ltd.	Juan Fantin	Google Inc.
Kevin Jacobs	DisplayLink (UK) Ltd.	Ken Wu	Google Inc.
Paulo Alcobia	DisplayLink (UK) Ltd.	Kyle Tso	Google Inc.
Peter Burgers	DisplayLink (UK) Ltd.	Mark Hayter	Google Inc.
Richard Petrie	DisplayLink (UK) Ltd.	Nathan Kolluru	Google Inc.
Chien-Cheng Kuo	eEver Technology, Inc.	Nithya Jagannathan	Google Inc.
Shyanjia Chen	eEver Technology, Inc.	Srikanth	Google Inc.
Abel Astley	Ellisys	Lakshmikanthan	
Chuck Trefts	Ellisys	Todd Broch	Google Inc.
Emmanuel Durin	Ellisys	Toshak Singhal	Google Inc.
Mario Pasquali	Ellisys	Vincent Palatin	Google Inc.
Tim Wei	Ellisys	Xuelin Wu	Google Inc.
Chien-Cheng Kuo	Etron Technology, Inc.	Zhenxue Xu	Google Inc.
Jack Yang	Etron Technology, Inc.	Alan Kinningham	Granite River Labs
Richard Crisp	Etron Technology, Inc.	Balamurugan	Granite River Labs
Shyanjia Chen	Etron Technology, Inc.	Manialagan	
TsungTa Lu	Etron Technology, Inc.	Mike Engbretson	Granite River Labs
Christian Klein	Fairchild Semiconductor	Mike Wu	Granite River Labs
Oscar Freitas	Fairchild Semiconductor	Mukesh Tatiya	Granite River Labs
Souhib Harb	Fairchild Semiconductor	Rajaraman V	Granite River Labs
Amanda Ying	Feature Integration Technology Inc.	Sivaram Murugesan	Granite River Labs
Jacky Chan	Feature Integration Technology Inc.	Tim Lin	Granite River Labs
Kenny Hsieh	Feature Integration Technology Inc.	Vishal Kakade	Granite River Labs
KungAn Lin	Feature Integration Technology Inc.	Alan Berkema	Hewlett Packard
Paul Yang	Feature Integration Technology Inc.	Lee Atkinson	Hewlett Packard
Su Jaden	Feature Integration Technology Inc.	Rahul Lakdawala	Hewlett Packard
Yu-Lin Chu	Feature Integration Technology Inc.	Robin Castell	Hewlett Packard
Yulin Lan	Feature Integration Technology Inc.	Ron Schooley	Hewlett Packard
AJ Yang	Foxconn / Hon Hai	Suketa Partiwalla	Hewlett Packard
Bob Hall	Foxconn / Hon Hai	Steve Chen	Hewlett Packard
Chihyin Kan	Foxconn / Hon Hai	Vaibhav Malik	Hewlett Packard
		Walter Fry	Hewlett Packard
		Hideyuki HAYAFUJI	Hosiden Corporation
		Keiji Mine	Hosiden Corporation
		Masaki Yamaoka	Hosiden Corporation
		Takashi Muto	Hosiden Corporation
		Yasunori Nishikawa	Hosiden Corporation
		Alan Berkema	HP Inc.

Kenneth Chan	HP Inc.	Venkataaramani	Intel Corporation
Lee Atkinson	HP Inc.	Gopalakrishnan	
Lee Leppo	HP Inc.	Ziv Kabiry	Intel Corporation
Rahul Lakdawala	HP Inc.	Jia Wei	Intersil Corporation
Robin Castell	HP Inc.	Al Hsiao	ITE Tech. Inc.
Roger Benson	HP Inc.	Greg Song	ITE Tech. Inc.
Steve Chen	HP Inc.	Richard Guo	ITE Tech. Inc.
Bai Sean	Huawei Technologies Co., Ltd.	Victor Lin	ITE Tech. Inc.
Chunjiang Zhao	Huawei Technologies Co., Ltd.	Y.C. Chou	ITE Tech. Inc.
JianQuan Wu	Huawei Technologies Co., Ltd.	Kenta Minejima	Japan Aviation Electronics Industry Ltd. (JAE)
Li Zongjian	Huawei Technologies Co., Ltd.	Mark Saubert	Japan Aviation Electronics Industry Ltd. (JAE)
Liansheng Zheng	Huawei Technologies Co., Ltd.	Toshio Shimoyama	Japan Aviation Electronics Industry Ltd. (JAE)
Lihua Duan	Huawei Technologies Co., Ltd.		
Min Chen	Huawei Technologies Co., Ltd.	Brian Fetz	Keysight Technologies Inc.
Wang Feng	Huawei Technologies Co., Ltd.	Jit Lim	Keysight Technologies Inc.
Wei Haihong	Huawei Technologies Co., Ltd.	Babu Mailachalam	Lattice Semiconductor Corp
James Xie	Hynetek Semiconductor Co., Ltd	Gianluca Mariani	Lattice Semiconductor Corp
Yingyang Ou	Hynetek Semiconductor Co., Ltd	Joel Coplen	Lattice Semiconductor Corp
Robert Heaton	Indie Semiconductor	Thomas Watza	Lattice Semiconductor Corp
Vincent Wang	Indie Semiconductor	Vesa Lauri	Lattice Semiconductor Corp
Benjamin Kropf	Infineon Technologies	Do Kyun Kim	LG electronics
Sie Boo Chiang	Infineon Technologies	Bruce Chuang	Leadtrend
Tue Fatt David Wee	Infineon Technologies	Eilian Liu	Leadtrend
Wee Tar Richard Ng	Infineon Technologies	Daniel H Jacobs	LeCroy Corporation
Wolfgang Furtner	Infineon Technologies	Jake Jacobs	LeCroy Corporation
Bob Dunstan	Intel Corporation	Kimberley McKay	LeCroy Corporation
Brad Saunders	Intel Corporation	Mike Engbretson	LeCroy Corporation
Chee Lim Nge	Intel Corporation	Mike Micheletti	LeCroy Corporation
Christine Krause	Intel Corporation	Roy Chestnut	LeCroy Corporation
Chuen Ming Tan	Intel Corporation	Tyler Joe	LeCroy Corporation
Dan Froelich	Intel Corporation	Phil Jakes	Lenovo
David Harriman	Intel Corporation	Aaron Melgar	Lion Semiconductor
David Hines	Intel Corporation	Chris Zhou	Lion Semiconductor
David Thompson	Intel Corporation	Sehyung Jeon	Lion Semiconductor
Guobin Liu	Intel Corporation	Wonyoung Kim	Lion Semiconductor
Harry Skinner	Intel Corporation	Yongho Kim	Lion Semiconductor
Henrik Leegaard	Intel Corporation	Dave Thompson	LSI Corporation
Jenn Chuan Cheng	Intel Corporation	Alan Kinningham	Luxshare-ICT
Jervis Lin	Intel Corporation	Alan Liu	Luxshare-ICT
John Howard	Intel Corporation	Daniel Chen	Luxshare-ICT
Karthi Vadivelu	Intel Corporation	Eric Wen	Luxshare-ICT
Leo Heiland	Intel Corporation	James Stevens	Luxshare-ICT
Maarit Harkonen	Intel Corporation	Josue Castillo	Luxshare-ICT
Nge Chee Lim	Intel Corporation	Pat Young	Luxshare-ICT
Paul Durley	Intel Corporation	Scott Shuey	Luxshare-ICT
Rahman Ismail	Intel Corporation	Chikara Kakizawa	Maxim Integrated Products
Rajaram Regupathy	Intel Corporation	Jacob Scott	Maxim Integrated Products
Ronald Swartz	Intel Corporation	Ken Helfrich	Maxim Integrated Products
Sarah Sharp	Intel Corporation	Michael Miskho	Maxim Integrated Products
Scott Brenden	Intel Corporation	Chris Yokum	MCCI Corporation
Sridharan	Intel Corporation	Geert Knapen	MCCI Corporation
Ranganathan		Terry Moore	MCCI Corporation
Steve McGowan	Intel Corporation	Velmurugan	MCCI Corporation
Tim McKee	Intel Corporation	Selvaraj	
Toby Opferman	Intel Corporation	Satoru Kumashiro	MegaChips Corporation
Uma Medepalli	Intel Corporation		

Brian Marley	Microchip Technology Inc.	Bart Vertenten	NXP Semiconductors
Dave Perchlik	Microchip Technology Inc.	Dennis Ha	NXP Semiconductors
Don Perkins	Microchip Technology Inc.	Dong Nguyen	NXP Semiconductors
Fernando Gonzalez	Microchip Technology Inc.	Guru Prasad	NXP Semiconductors
John Sisto	Microchip Technology Inc.	Ken Jaramillo	NXP Semiconductors
Josh Averyt	Microchip Technology Inc.	Krishnan TN	NXP Semiconductors
Kiet Tran	Microchip Technology Inc.	Michael Joehren	NXP Semiconductors
Mark Bohm	Microchip Technology Inc.	Robert de Nie	NXP Semiconductors
Matthew Kalibat	Microchip Technology Inc.	Rod Whitby	NXP Semiconductors
Mick Davis	Microchip Technology Inc.	Vijendra Kuroodi	NXP Semiconductors
Prasanna	Microchip Technology Inc.	Winston Langeslag	NXP Semiconductors
Vengateshan		Robert Heaton	Obsidian Technology
Rich Wahler	Microchip Technology Inc.	Andrew Yoo	ON Semiconductor
Richard Petrie	Microchip Technology Inc.	Brady Maasen	ON Semiconductor
Ronald Kunin	Microchip Technology Inc.	Bryan McCoy	ON Semiconductor
Shannon Cash	Microchip Technology Inc.	Christian Klein	ON Semiconductor
Thomas Farkas	Microchip Technology Inc.	Cor Voorwinden	ON Semiconductor
Venkataraman	Microchip Technology Inc.	Edward Berrios	ON Semiconductor
Krishnamoorthy		Michael Smith	ON Semiconductor
Andrew Yang	Microsoft Corporation	Oscar Freitas	ON Semiconductor
Anthony Chen	Microsoft Corporation	Tom Duffy	ON Semiconductor
Arvind Murching	Microsoft Corporation	Brian Collins	Parade Technologies Inc.
Dave Perchlik	Microsoft Corporation	Craig Wiley	Parade Technologies Inc.
David Voth	Microsoft Corporation	Aditya Kulkarni	Power Integrations
Geoff Shew	Microsoft Corporation	Akshay Nayaknur	Power Integrations
Jayson Kastens	Microsoft Corporation	Amruta Patra	Power Integrations
Kai Inha	Microsoft Corporation	Rahul Joshi	Power Integrations
Marwan Kadado	Microsoft Corporation	Ricardo Pregiteer	Power Integrations
Michelle Bergeron	Microsoft Corporation	Shruti Anand	Power Integrations
Nathan Sherman	Microsoft Corporation	Amit gupta	Qualcomm, Inc
Rahul Ramadas	Microsoft Corporation	George Paparrizos	Qualcomm, Inc
Randy Aull	Microsoft Corporation	Giovanni Garcea	Qualcomm, Inc
Shiu Ng	Microsoft Corporation	Jack Pham	Qualcomm, Inc
Tieyong Yin	Microsoft Corporation	James Goel	Qualcomm, Inc
Timo Toivola	Microsoft Corporation	Joshua Warner	Qualcomm, Inc
Toby Nixon	Microsoft Corporation	Karyn Vuong	Qualcomm, Inc
Vahid Vassey	Microsoft Corporation	Lalan Mishra	Qualcomm, Inc
Vivek Gupta	Microsoft Corporation	Vamsi Samavedam	Qualcomm, Inc
Yang You	Microsoft Corporation	Vatsal Patel	Qualcomm, Inc
Adib Al Abaji	Molex LLC	Chris Sporck	Qualcomm, Inc.
Aaron Xu	Monolithic Power Systems Inc.	Craig Aiken	Qualcomm, Inc.
Bo Zhou	Monolithic Power Systems Inc.	Narendra Mehta	Qualcomm, Inc.
Christian Sporck	Monolithic Power Systems Inc.	Terry Remple	Qualcomm, Inc.
Di Han	Monolithic Power Systems Inc.	Will Kun	Qualcomm, Inc.
Zhihong Yu	Monolithic Power Systems Inc.	Yoram Rimoni	Qualcomm, Inc.
Dan Wagner	Motorola Mobility Inc.	Fan-Hau Hsu	Realtek Semiconductor Corp.
Ben Crowe	MQP Electronics Ltd.	Tsung-Peng Chuang	Realtek Semiconductor Corp.
Pat Crowe	MQP Electronics Ltd.	Atsushi Mitamura	Renesas Electronics Corp.
Sten Carlsen	MQP Electronics Ltd.	Bob Dunstan	Renesas Electronics Corp.
Kenji Oguma	NEC Corporation	Brian Allen	Renesas Electronics Corp.
Frank Borngräber	Nokia Corporation	Dan Aoki	Renesas Electronics Corp.
Kai Inha	Nokia Corporation	Hajime Nozaki	Renesas Electronics Corp.
Pekka Leinonen	Nokia Corporation	John Carpenter	Renesas Electronics Corp.
Richard Petrie	Nokia Corporation	Kiichi Muto	Renesas Electronics Corp.
Sten Carlsen	Nokia Corporation	Masami Katagiri	Renesas Electronics Corp.
Abhijeet Kulkarni	NXP Semiconductors	Nobuo Furuya	Renesas Electronics Corp.
Ahmad Yazdi	NXP Semiconductors		

Patrick Yu	Renesas Electronics Corp.	Shannon Cash	SMSC
Peter Teng	Renesas Electronics Corp.	Tim Knowlton	SMSC
Philip Leung	Renesas Electronics Corp.	William Chiechi	SMSC
Steve Roux	Renesas Electronics Corp.	Shigenori Tagami	Sony Corporation
Tetsu Sato	Renesas Electronics Corp.	Shinichi Hirata	Sony Corporation
Toshifumi Yamaoka	Renesas Electronics Corp.	Amanda Hosler	Specwerkz
Chunan Kuo	Richtek Technology Corporation	Bob Dunstan	Specwerkz
Heinz Wei	Richtek Technology Corporation	Diane Lenox	Specwerkz
TZUHSIEN CHUANG	Richtek Technology Corporation	Michael Munn	StarTech.com Ltd.
Tatsuya Irisawa	Ricoh Company Ltd.	Fabien Friess	ST-Ericsson
Akihiro Ono	Rohm Co. Ltd.	Giuseppe Platania	ST-Ericsson
Chris Lin	Rohm Co. Ltd.	Jean-Francois Gatto	ST-Ericsson
Hidenori Nishimoto	Rohm Co. Ltd.	Milan Stamenkovic	ST-Ericsson
Kris Bahar	Rohm Co. Ltd.	Nicolas Florenchie	ST-Ericsson
Manabu Miyata	Rohm Co. Ltd.	Patrizia Milazzo	ST-Ericsson
Ruben Balbuena	Rohm Co. Ltd.	Christophe Cochard	STMicroelectronics
Takashi Sato	Rohm Co. Ltd.	Christophe Lorin	STMicroelectronics
Vijendra Kuroodi	Rohm Co. Ltd.	Filippo Bonaccorso	STMicroelectronics
Yusuke Kondo	Rohm Co. Ltd.	Jessy Guilbot	STMicroelectronics
Kazuomi Nagai	ROHM Co., Ltd.	Joel Huloux	STMicroelectronics
Matti Kulmala	Salcomp Plc	John Bloomfield	STMicroelectronics
Toni Lehimo	Salcomp Plc	Massimo Panzica	STMicroelectronics
Tong Kim	Samsung Electronics Co. Ltd.	Meriem Mersel	STMicroelectronics
Alvin Cox	Seagate Technology LLC	Nathalie Ballot	STMicroelectronics
Emmanuel Lemay	Seagate Technology LLC	Pascal Legrand	STMicroelectronics
John Hein	Seagate Technology LLC	Patrizia Milazzo	STMicroelectronics
Marc Noblitt	Seagate Technology LLC	Richard O'Connor	STMicroelectronics
Michael Morgan	Seagate Technology LLC	Morten Christiansen	Synopsys, Inc.
Ronald Rueckert	Seagate Technology LLC	Nivin George	Synopsys, Inc.
Tony Priborsky	Seagate Technology LLC	Zongyao Wen	Synopsys, Inc.
Chin Chang	Semtech Corporation	Joan Marrinan	Tektronix
Tom Farkas	Semtech Corporation	Kimberley McKay	Teledyne-LeCroy
Ning Dai	Silergy Corp.	Matthew Dunn	Teledyne-LeCroy
Wanfeng Zhang	Silergy Corp.	Tony Minchell	Teledyne-LeCroy
Kafai Leung	Silicon Laboratories, Inc.	Anand Dabak	Texas Instruments
Kok Hong Soh	Silicon Laboratories, Inc.	Bill Waters	Texas Instruments
Sorin Badiu	Silicon Laboratories, Inc.	Bing Lu	Texas Instruments
Steven Ghang	Silicon Laboratories, Inc.	Deric Waters	Texas Instruments
Abhishek Sardeshpande	SiliConch Systems Private Limited	Grant Ley	Texas Instruments
Aniket Mathad	SiliConch Systems Private Limited	Gregory Watkins	Texas Instruments
Chandana N	SiliConch Systems Private Limited	Ingolf Frank	Texas Instruments
Jaswanth Ammineni	SiliConch Systems Private Limited	Ivo Huber	Texas Instruments
Jinisha Patel	SiliConch Systems Private Limited	Javed Ahmad	Texas Instruments
Kaustubh Kumar	SiliConch Systems Private Limited	Jean Picard	Texas Instruments
Nitish	SiliConch Systems Private Limited	John Perry	Texas Instruments
Pavitra	SiliConch Systems Private Limited	Martin Patoka	Texas Instruments
Balasubramanian	SiliConch Systems Private Limited	Mike Campbell	Texas Instruments
Rakesh Polasa	SiliConch Systems Private Limited	Scott Jackson	Texas Instruments
Satish Anand	SiliConch Systems Private Limited	Shafiuddin	Texas Instruments
Verkila		Mohammed	
Shubham Paliwal	SiliConch Systems Private Limited	Srinath Hosur	Texas Instruments
Vishnu Pusuluri	SiliConch Systems Private Limited	Steven Tom	Texas Instruments
John Sisto	SMSC	Yoon Lee	Texas Instruments
Ken Gay	SMSC	Tim Wilhelm	The Silanna Group Pty. Ltd.
Mark Bohm	SMSC	Tod Wolf	The Silanna Group Pty. Ltd.
Richard Wahler	SMSC	Chris Yokum	Total Phase
		Eric Wall	UL LLC

Jason Smith	UL LLC
Steven Chen	Unigraf OY
Topi Lampiranta	Unigraf OY
Brad Cox	Ventev Mobile
Colin Vose	Ventev Mobile
Dydron Lin	VIA Technologies, Inc.
Fong-Jim Wang	VIA Technologies, Inc.
Jay Tseng	VIA Technologies, Inc.
Rex Chang	VIA Technologies, Inc.
Terrance Shih	VIA Technologies, Inc.
Ho Wen Tsai	Weltrend Semiconductor
Hung Chiang	Weltrend Semiconductor
Jeng Cheng Liu	Weltrend Semiconductor
Priscilla Lee	Weltrend Semiconductor
Wayne Lo	Weltrend Semiconductor
Charles Neumann	Western Digital Technologies, Inc.
Curtis Stevens	Western Digital Technologies, Inc.
John Maroney	Western Digital Technologies, Inc.
Joe O'Brien	Wilder Technologies
Will Miller	Wilder Technologies
Juejia Zhou	Xiaomi Communications Co., Ltd.
Xiaoxing Yang	Xiaomi Communications Co., Ltd.

## Revision History

Revision	Version	Comments	Issue Date
1.0	1.0	Initial release Revision 1.0	5 July, 2012
1.0	1.1	Including errata through 31-October-2012	31 October 2012
1.0	1.2	Including errata through 26-June-2013	26 June, 2013
1.0	1.3	Including errata through 11-March-2014	11 March 2014
2.0	1.0	Initial release Revision 2.0	11 August 2014
2.0	1.1	Including errata through 7-May 2015	7 May 2015
2.0	1.2	Including errata through 25-March-2016	25 March 2016
2.0	1.3	Including errata through 11-January-2017	11 January 2017
3.0	1.0	Initial release Revision 3.0	11 December 2015
3.0	1.0a	Including errata through 25-March-2016	25 March 2016
3.0	1.1	Including errata through 12-January-2016	12 January 2017
3.0	1.2	Including errata through 21-June-2018	21 June 2018
3.0	2.0	Including errata through 29-August-2019	29 August 2019
3.1	1.0	Including errata through May 2021	May 2021
3.1	1.1	Including errata through July 2021	July 2021

## Table of Contents

INTELLECTUAL PROPERTY DISCLAIMER .....	6
Chairs .....	7
Editors .....	7
Contributors .....	7
Revision History .....	14
Table of Contents .....	15
List of Tables .....	35
List of Figures .....	42
1. Introduction .....	51
1.1 Overview .....	51
1.2 Purpose .....	52
1.3 Scope .....	52
1.4 Conventions .....	53
1.4.1 Precedence .....	53
1.4.2 Keywords .....	53
1.4.2.1 Conditional Normative .....	53
1.4.2.2 Deprecated .....	53
1.4.2.3 Discarded .....	53
1.4.2.4 Ignored .....	53
1.4.2.5 Invalid .....	53
1.4.2.6 May .....	53
1.4.2.7 May Not .....	53
1.4.2.8 N/A .....	53
1.4.2.9 Optional/Optionally/Optional Normative .....	54
1.4.2.10 Reserved .....	54
1.4.2.11 Shall/Normative .....	54
1.4.2.12 Shall Not .....	54
1.4.2.13 Should .....	54
1.4.2.14 Should Not .....	54
1.4.2.15 Valid .....	54
1.4.3 Numbering .....	54
1.5 Related Documents .....	54
1.6 Terms and Abbreviations .....	55
1.7 Parameter Values .....	63
1.8 Changes from Revision 3.0 .....	64
1.9 Compatibility with Revision 2.0 .....	64
2. Overview .....	64
2.1 Introduction .....	64
2.2 Section Overview .....	65
2.3 Compatibility with Revision 2.0 .....	66
2.4 USB Power Delivery Capable Devices .....	66
2.5 SOP* Communication .....	67
2.5.1 Introduction .....	67
2.5.2 SOP* Collision Avoidance .....	67



2.5.3	SOP Communication.....	67
2.5.4	SOP'/SOP'' Communication with Cable Plugs .....	67
2.6	Operational Overview .....	69
2.6.1	Source Operation .....	69
2.6.2	Sink Operation.....	72
2.6.3	Cable Plugs .....	74
2.7	Architectural Overview .....	75
2.7.1	Policy .....	77
2.7.1.1	System Policy Manager.....	77
2.7.1.2	Device Policy Manager.....	78
2.7.1.3	Policy Engine .....	78
2.7.2	Message Formation and Transmission.....	78
2.7.2.1	Protocol Layer.....	78
2.7.2.2	PHY Layer .....	78
2.7.3	Collision Avoidance .....	78
2.7.3.1	Policy Engine .....	78
2.7.3.2	Protocol Layer.....	78
2.7.3.3	PHY Layer .....	79
2.7.4	Power supply .....	79
2.7.4.1	Source .....	79
2.7.4.2	Sink .....	79
2.7.4.3	Dual-Role Power Ports.....	79
2.7.4.4	Dead Battery or Lost Power Detection.....	79
2.7.4.5	VCONN Source.....	79
2.7.5	DFP/UFP .....	79
2.7.5.1	Downstream Facing Port (DFP).....	79
2.7.5.2	Upstream Facing Port (UFP) .....	79
2.7.5.3	Dual-Role Data Ports .....	80
2.7.6	Cable and Connectors .....	80
2.7.6.1	USB-C Port Control.....	80
2.7.7	Interactions between Non-PD, BC and PD devices .....	80
2.7.8	Power Rules .....	80
2.8	Extended Power Range (EPR) Operation .....	80
2.9	Charging Models .....	82
2.9.1	Fixed Voltage Charging Models .....	82
2.9.2	Programmable Power Supply (PPS) Charging Models .....	83
2.9.3	Adjustable Voltage Supply (AVS) Charging Models.....	83
3.	USB Type-A and USB Type-B Cable Assemblies and Connectors .....	83
4.	Electrical Requirements.....	83
4.1	Interoperability with other USB Specifications .....	83
4.2	Dead Battery Detection / Unpowered Port Detection.....	84
4.3	Cable IR Ground Drop (IR Drop) .....	84
4.4	Cable Type Detection .....	84
5.	Physical Layer .....	84
5.1	Physical Layer Overview .....	84
5.2	Physical Layer Functions.....	84
5.3	Symbol Encoding .....	86
5.4	Ordered Sets.....	87
5.5	Transmitted Bit Ordering .....	88



5.6	Packet Format	89
5.6.1	Packet Framing	89
5.6.1.1	Preamble	89
5.6.1.2	Start of Packet Sequences	89
5.6.1.2.1	Start of Packet Sequence (SOP)	89
5.6.1.2.2	Start of Packet Sequence Prime (SOP')	90
5.6.1.2.3	Start of Packet Sequence Double Prime (SOP'')	90
5.6.1.2.4	Start of Packet Sequence Prime Debug (SOP'_Debug)	90
5.6.1.2.5	Start of Packet Sequence Double Prime Debug (SOP''_Debug)	91
5.6.1.3	Packet Payload	91
5.6.1.4	CRC	91
5.6.1.5	End of Packet (EOP)	91
5.6.2	CRC	91
5.6.3	Packet Detection Errors	93
5.6.4	Hard Reset	93
5.6.5	Cable Reset	94
5.7	Collision Avoidance	94
5.8	Biphase Mark Coding (BMC) Signaling Scheme	95
5.8.1	Encoding and signaling	95
5.8.2	Transmit and Receive Masks	98
5.8.2.1	Transmit Masks	98
5.8.2.2	Receive Masks	100
5.8.3	Transmitter Load Model	104
5.8.4	BMC Common specifications	105
5.8.4.1	BMC Common Parameters	106
5.8.5	BMC Transmitter Specifications	106
5.8.5.1	Capacitance when not transmitting	107
5.8.5.2	Source Output Impedance	107
5.8.5.3	Bit Rate Drift	107
5.8.5.4	Inter-Frame Gap	108
5.8.5.5	Shorting of Transmitter Output	108
5.8.5.6	Fast Role Swap Transmission	108
5.8.6	BMC Receiver Specifications	109
5.8.6.1	Definition of Idle	109
5.8.6.2	Multi-Drop	110
5.8.6.3	Fast Role Swap Detection	110
5.9	Built in Self-Test (BIST)	112
5.9.1	BIST Carrier Mode	112
5.9.2	BIST Test Data	112
6.	Protocol Layer	112
6.1	Overview	112
6.2	Messages	112
6.2.1	Message Construction	113
6.2.1.1	Message Header	114
6.2.1.1.1	Extended	114
6.2.1.1.2	Number of Data Objects	114
6.2.1.1.3	MessageID	114

6.2.1.1.4	Port Power Role.....	115
6.2.1.1.5	Specification Revision.....	115
6.2.1.1.6	Port Data Role .....	117
6.2.1.1.7	Cable Plug .....	117
6.2.1.1.8	Message Type .....	117
6.2.1.2	Extended Message Header .....	118
6.2.1.2.1	Chunked .....	118
6.2.1.2.2	Chunk Number .....	119
6.2.1.2.3	Request Chunk .....	119
6.2.1.2.4	Data Size .....	119
6.2.1.2.5	Extended Message Examples .....	119
6.3	Control Message .....	124
6.3.1	GoodCRC Message .....	125
6.3.2	GotoMin Message.....	125
6.3.3	Accept Message .....	125
6.3.4	Reject Message .....	126
6.3.5	Ping Message.....	126
6.3.6	PS_RDY Message .....	126
6.3.7	Get_Source_Cap Message .....	126
6.3.8	Get_Sink_Cap Message .....	126
6.3.9	DR_Swap Message .....	127
6.3.10	PR_Swap Message.....	127
6.3.11	VCONN_Swap Message .....	128
6.3.12	Wait Message.....	128
6.3.12.1	Wait in response to a Request Message .....	129
6.3.12.2	Wait in response to a PR_Swap Message .....	129
6.3.12.3	Wait in response to a DR_Swap Message .....	129
6.3.12.4	Wait in response to a VCONN_Swap Message.....	129
6.3.13	Soft Reset Message .....	130
6.3.14	Data_Reset Message.....	130
6.3.15	Data_Reset_Complete Message .....	131
6.3.16	Not_Supported Message .....	131
6.3.17	Get_Source_Cap_Extended Message.....	131
6.3.18	Get_Status Message .....	131
6.3.19	FR_Swap Message.....	131
6.3.20	Get_PPS_Status.....	132
6.3.21	Get_Country_Codes .....	132
6.3.22	Get_Sink_Cap_Extended Message .....	132
6.3.23	Get_Source_Info Message.....	132
6.3.24	Get_Revision Message .....	132
6.4	Data Message .....	132
6.4.1	Capabilities Message.....	133
6.4.1.1	Use of the Capabilities Message .....	135
6.4.1.1.1	Use by Sources .....	135
6.4.1.1.2	Use by Sinks.....	135
6.4.1.1.3	Use by Dual-Role Power devices .....	135
6.4.1.2	Source_Capabilities Message .....	135
6.4.1.2.1	Management of the Power Reserve .....	136
6.4.1.2.2	Fixed Supply Power Data Object.....	137

6.4.1.2.3	Variable Supply (non-Battery) Power Data Object.....	139
6.4.1.2.4	Battery Supply Power Data Object.....	139
6.4.1.2.5	Augmented Power Data Object (APDO) .....	140
6.4.1.3	Sink Capabilities Message .....	141
6.4.1.3.1	Sink Fixed Supply Power Data Object.....	141
6.4.1.3.2	Variable Supply (non-Battery) Power Data Object.....	143
6.4.1.3.3	Battery Supply Power Data Object .....	143
6.4.1.3.4	Programmable Power Supply Augmented Power Data Object .....	143
6.4.2	Request Message .....	144
6.4.2.1	Object Position.....	146
6.4.2.2	GiveBack Flag.....	146
6.4.2.3	Capability Mismatch .....	146
6.4.2.4	USB Communications Capable .....	147
6.4.2.5	No USB Suspend .....	147
6.4.2.6	Unchunked Extended Messages Supported .....	147
6.4.2.7	EPR Mode Capable.....	147
6.4.2.8	Operating Current .....	148
6.4.2.9	Maximum Operating Current .....	148
6.4.2.10	Minimum Operating Current .....	148
6.4.2.11	Operating Power .....	149
6.4.2.12	Maximum Operating Power .....	149
6.4.2.13	Minimum Operating Power .....	149
6.4.2.14	Output Voltage.....	149
6.4.3	BIST Message .....	149
6.4.3.1	BIST Carrier Mode .....	151
6.4.3.2	BIST Test Data .....	151
6.4.3.3	BIST Shared Capacity Test Mode .....	151
6.4.3.3.1	BIST Shared Test Mode Entry.....	151
6.4.3.3.2	BIST Shared Test Mode Exit.....	151
6.4.4	Vendor Defined Message.....	152
6.4.4.1	Unstructured VDM.....	153
6.4.4.1.1	USB Vendor ID .....	153
6.4.4.1.2	VDM Type.....	153
6.4.4.2	Structured VDM .....	153
6.4.4.2.1	SVID .....	155
6.4.4.2.2	VDM Type.....	155
6.4.4.2.3	Structured VDM Version .....	155
6.4.4.2.4	Object Position .....	155
6.4.4.2.5	Command Type .....	156
6.4.4.2.6	Command .....	156
6.4.4.3	Use of Commands.....	157
6.4.4.3.1	Discover Identity .....	157
6.4.4.3.2	Discover SVIDs.....	172
6.4.4.3.3	Discover Modes .....	173
6.4.4.3.4	Enter Mode Command .....	174
6.4.4.3.5	Exit Mode Command.....	176
6.4.4.3.6	Attention .....	177

6.4.4.4	Command Processes .....	177
6.4.4.4.1	Discovery Process .....	178
6.4.4.4.2	Enter Vendor Mode / Exit Vendor Mode Processes .....	179
6.4.4.5	VDM Message Timing and Normal PD Messages .....	180
6.4.5	Battery_Status Message .....	180
6.4.5.1	Battery Present Capacity .....	181
6.4.5.2	Battery Info .....	181
6.4.5.2.1	Invalid Battery Reference .....	181
6.4.5.2.2	Battery is Present .....	181
6.4.5.2.3	Battery Charging Status .....	181
6.4.6	Alert Message .....	181
6.4.6.1	Type of Alert .....	182
6.4.6.1.1	Battery Status Change .....	182
6.4.6.1.2	Over-Current Protection Event .....	182
6.4.6.1.3	Over-Temperature Protection Event .....	182
6.4.6.1.4	Operating Condition Change .....	182
6.4.6.1.5	Source Input Change Event .....	182
6.4.6.1.6	Over-Voltage Protection Event .....	183
6.4.6.1.7	Extended Alert Event .....	183
6.4.6.2	Fixed Batteries .....	183
6.4.6.3	Hot Swappable Batteries .....	183
6.4.6.4	Extended Alert Event Types .....	183
6.4.6.4.1	Power State Change .....	183
6.4.6.4.2	Power Button Press .....	183
6.4.6.4.3	Power Button Release .....	183
6.4.6.4.4	Controller initiated wake .....	183
6.4.7	Get_Country_Info Message .....	183
6.4.8	Enter_USB Message .....	184
6.4.8.1	USB Mode Field .....	185
6.4.8.2	USB4 DRD Field .....	185
6.4.8.3	USB3 DRD Field .....	185
6.4.8.4	Cable Speed Field .....	185
6.4.8.5	Cable Type Field .....	185
6.4.8.6	Cable Current Field .....	185
6.4.8.7	PCIe Support Field .....	186
6.4.8.8	DP Support Field .....	186
6.4.8.9	TBT Support Field .....	186
6.4.8.10	Host Present Field .....	186
6.4.9	EPR_Request Message .....	186
6.4.10	EPR_Mode Message .....	186
6.4.10.1	Process to enter EPR Mode .....	187
6.4.10.2	Operation in EPR Mode .....	190
6.4.10.3	Exiting EPR Mode .....	190
6.4.10.3.1	Commanded Exit .....	190
6.4.10.3.2	Implicit Exit .....	190
6.4.10.3.3	Exits due to errors .....	191
6.4.11	Source_Info Message .....	191
6.4.11.1	Port Type Field .....	191

6.4.11.2	Port Maximum PDP Field .....	191
6.4.11.3	Port Present PDP Field .....	192
6.4.11.4	Port Reported PDP Field .....	192
6.4.12	Revision Message .....	192
6.5	Extended Message .....	192
6.5.1	Source_Capabilities_Extended Message .....	193
6.5.1.1	Vendor ID (VID) Field .....	195
6.5.1.2	Product ID (PID) Field .....	196
6.5.1.3	XID Field .....	196
6.5.1.4	Firmware Version Field .....	196
6.5.1.5	Hardware Version Field .....	196
6.5.1.6	Voltage Regulation Field .....	196
6.5.1.6.1	Load Step Slew Rate .....	196
6.5.1.6.2	Load Step Magnitude .....	196
6.5.1.7	Holdup Time Field .....	196
6.5.1.8	Compliance Field .....	196
6.5.1.9	Touch Current Field .....	196
6.5.1.10	Peak Current Field .....	197
6.5.1.11	Touch Temp Field .....	197
6.5.1.12	Source Inputs Field .....	197
6.5.1.13	Number of Batteries/Battery Slots Field .....	197
6.5.1.14	SPR Source PDP Rating Field .....	198
6.5.1.15	EPR Source PDP Rating Field .....	198
6.5.2	Status Message .....	198
6.5.2.1	SOP Status Message .....	198
6.5.2.1.1	Internal Temp Field .....	200
6.5.2.1.2	Present Input Field .....	200
6.5.2.1.3	Present Battery Input Field .....	200
6.5.2.1.4	Event Flags Field .....	200
6.5.2.1.5	Temperature Status Field .....	201
6.5.2.1.6	Power Status Field .....	201
6.5.2.1.7	Power state change .....	201
6.5.2.2	SOP'/SOP'' Status Message .....	201
6.5.2.2.1	Internal Temp Field .....	202
6.5.2.2.2	Thermal Shutdown Field .....	202
6.5.3	Get_Battery_Cap Message .....	202
6.5.4	Get_Battery_Status Message .....	203
6.5.5	Battery_Capabilities Message .....	203
6.5.5.1	Battery Design Capacity Field .....	204
6.5.5.2	Battery Last Full Charge Capacity Field .....	204
6.5.5.3	Battery Type Field .....	204
6.5.5.3.1	Invalid Battery Reference .....	204
6.5.6	Get_Manufacturer_Info Message .....	204
6.5.7	Manufacturer_Info Message .....	205
6.5.7.1	Vendor ID (VID) .....	205
6.5.7.2	Product ID (PID) .....	205
6.5.7.3	Manufacturer String .....	206
6.5.8	Security Messages .....	206
6.5.8.1	Security_Request .....	206

6.5.8.2	Security_Response .....	206
6.5.9	Firmware Update Messages .....	207
6.5.9.1	Firmware_Update_Request .....	207
6.5.9.2	Firmware_Update_Response .....	207
6.5.10	PPS_Status Message .....	207
6.5.10.1	Output Voltage Field .....	208
6.5.10.2	Output Current Field .....	208
6.5.10.3	Real Time Flags Field .....	208
6.5.11	Country_Codes Message .....	208
6.5.11.1	Country Code Field .....	209
6.5.12	Country_Info Message .....	209
6.5.12.1	Country Code Field .....	209
6.5.12.2	Country Specific Data Field .....	209
6.5.13	Sink_Capabilities_Extended Message .....	210
6.5.13.1	Vendor ID (VID) Field .....	212
6.5.13.2	Product ID (PID) Field .....	212
6.5.13.3	XID Field .....	212
6.5.13.4	Firmware Version Field .....	212
6.5.13.5	Hardware Version Field .....	212
6.5.13.6	SKEDB Version Field .....	212
6.5.13.7	Load Step Field .....	212
6.5.13.8	Sink Load Characteristics Field .....	212
6.5.13.9	Compliance Field .....	212
6.5.13.10	Touch Temp .....	212
6.5.13.11	Battery Info .....	212
6.5.13.12	Sink Modes .....	213
6.5.13.13	Sink Minimum PDP .....	213
6.5.13.14	Sink Operational PDP .....	213
6.5.13.15	Sink Maximum PDP .....	213
6.5.13.16	EPR Sink Minimum PDP .....	213
6.5.13.17	EPR Sink Operational PDP .....	213
6.5.13.18	EPR Sink Maximum PDP .....	214
6.5.14	Extended_Control Message .....	214
6.5.14.1	EPR_Get_Source_Cap Message .....	214
6.5.14.2	EPR_Get_Sink_Cap Message .....	215
6.5.14.3	EPR_KeepAlive Message .....	215
6.5.14.4	EPR_KeepAlive_Ack Message .....	215
6.5.15	EPR Capabilities Message .....	215
6.5.15.1	EPR Capabilities Message Construction .....	215
6.5.15.2	EPR_Source_Capabilities Message .....	216
6.5.15.3	EPR_Sink_Capabilities Message .....	216
6.5.16	Vendor_Defined_Extended Message .....	216
6.6	Timers .....	217
6.6.1	CRCReceiveTimer .....	217
6.6.2	SenderResponseTimer .....	218
6.6.3	Capability Timers .....	218
6.6.3.1	SourceCapabilityTimer .....	218
6.6.3.2	SinkWaitCapTimer .....	218
6.6.3.3	tFirstSourceCap .....	219

6.6.4	Wait Timers and Times .....	219
6.6.4.1	SinkRequestTimer .....	219
6.6.4.2	tPRSwapWait .....	219
6.6.4.3	tDRSwapWait .....	219
6.6.4.4	tVconnSwapWait .....	219
6.6.5	Power Supply Timers .....	220
6.6.5.1	PSTransitionTimer .....	220
6.6.5.2	PSSourceOffTimer .....	220
6.6.5.2.1	Use during Power Role Swap .....	220
6.6.5.2.2	Use during Fast Role Swap .....	220
6.6.5.3	PSSourceOnTimer .....	221
6.6.5.3.1	Use during Power Role Swap .....	221
6.6.5.3.2	Use during Fast Role Swap .....	221
6.6.6	NoResponseTimer .....	221
6.6.7	BIST Timers .....	222
6.6.7.1	tBISTCarrierMode .....	222
6.6.7.2	BISTContModeTimer .....	222
6.6.7.3	tBISTSharedTestMode .....	222
6.6.8	Power Role Swap Timers .....	222
6.6.8.1	SwapSourceStartTimer .....	222
6.6.9	Soft Reset Timers .....	222
6.6.9.1	tSoftReset .....	222
6.6.9.2	tProtErrSoftReset .....	222
6.6.10	Data Reset Timers .....	222
6.6.10.1	VCONNDischargeTimer .....	222
6.6.10.2	tDataReset .....	223
6.6.10.3	DataResetFailTimer .....	223
6.6.11	Hard Reset Timers .....	223
6.6.11.1	HardResetCompleteTimer .....	223
6.6.11.2	PSHardResetTimer .....	223
6.6.11.3	tDRSwapHardReset .....	223
6.6.11.4	tProtErrHardReset .....	223
6.6.12	Structured VDM Timers .....	224
6.6.12.1	VDMResponseTimer .....	224
6.6.12.2	VDMModeEntryTimer .....	224
6.6.12.3	VDMModeExitTimer .....	224
6.6.12.4	tVDMBusy .....	225
6.6.13	VCONN Timers .....	225
6.6.13.1	VCONNOnTimer .....	225
6.6.13.2	tVCONNSourceOff .....	225
6.6.14	tCableMessage .....	225
6.6.15	DiscoverIdentityTimer .....	225
6.6.16	Collision Avoidance Timers .....	225
6.6.17	Fast Role Swap Timers .....	226
6.6.17.1	tFRSwap5V .....	226
6.6.17.2	tFRSwapComplete .....	226
6.6.17.3	tFRSwapInit .....	226
6.6.18	Chunking Timers .....	226
6.6.18.1	ChunkingNotSupportedTimer .....	226

6.6.18.2	ChunkSenderRequestTimer .....	226
6.6.18.3	ChunkSenderResponseTimer.....	226
6.6.19	Programmable Power Supply Timers .....	227
6.6.19.1	SinkPPSPeriodicTimer .....	227
6.6.19.2	SourcePPSCmmTimer.....	227
6.6.20	tEnterUSB .....	227
6.6.21	EPR Timers .....	228
6.6.21.1	SinkEPREnterTimer Timer .....	228
6.6.21.2	SinkEPRKeepAlive Timer.....	228
6.6.21.3	SourceEPRKeepAlive Timer.....	228
6.6.22	Time Values and Timers .....	228
6.7	Counters .....	232
6.7.1	MessageID Counter .....	232
6.7.1.1	Transmitter Usage .....	232
6.7.1.2	Receiver Usage .....	232
6.7.2	Retry Counter .....	232
6.7.3	Hard Reset Counter .....	233
6.7.4	Capabilities Counter .....	233
6.7.5	Discover Identity Counter .....	233
6.7.6	VDMBusyCounter .....	233
6.7.7	Counter Values and Counters .....	233
6.8	Reset .....	234
6.8.1	Soft Reset and Protocol Error .....	234
6.8.2	Data Reset .....	236
6.8.3	Hard Reset .....	236
6.8.3.1	Cable Plugs and Hard Reset .....	237
6.8.3.2	Modal Operation and Hard Reset .....	237
6.8.4	Cable Reset.....	237
6.9	Collision Avoidance .....	237
6.10	Message Discarding .....	237
6.11	State behavior .....	239
6.11.1	Introduction to state diagrams used in Chapter 6 .....	239
6.11.2	State Operation .....	239
6.11.2.1	Protocol Layer Chunking .....	240
6.11.2.1.1	Architecture of Device Including Chunking Layer .....	240
6.11.2.1.2	Chunked Rx State Diagram.....	242
6.11.2.1.3	Chunked Tx State Diagram .....	245
6.11.2.1.4	Chunked Message Router State Diagram.....	249
6.11.2.2	Protocol Layer Message Transmission .....	251
6.11.2.2.1	Common Protocol Layer Message Transmission State Diagram.....	251
6.11.2.2.2	Source Protocol Layer Message Transmission State Diagram.....	254
6.11.2.2.3	Sink Protocol Layer Message Transmission State Diagram.....	255
6.11.2.3	Protocol Layer Message Reception .....	256
6.11.2.3.1	PRL_Rx_Wait_for_PHY_Message state .....	257
6.11.2.3.2	PRL_Rx_Layer_Reset_for_Receive state.....	257
6.11.2.3.3	PRL_Rx_Send_GoodCRC state .....	258
6.11.2.3.4	PRL_Rx_Check_MessageID state.....	258



6.11.2.3.5	PRL_Rx_Store_MessageID state .....	258
6.11.2.4	Hard Reset operation .....	259
6.11.2.4.1	PRL_HR_Reset_Layer state .....	260
6.11.2.4.2	PRL_HR_Indicate_Hard_Reset state .....	260
6.11.2.4.3	PRL_HR_Request_Hard_Reset state .....	260
6.11.2.4.4	PRL_HR_Wait_for_PHY_Hard_Reset_Complete state .....	260
6.11.2.4.5	PRL_HR_PHY_Hard_Reset_Requested state .....	261
6.11.2.4.6	PRL_HR_Wait_for_PE_Hard_Reset_Complete state .....	261
6.11.2.4.7	PRL_HR_PE_Hard_Reset_Complete .....	261
6.11.3	List of Protocol Layer States .....	262
6.12	Message Applicability .....	264
6.12.1	Applicability of Control Messages .....	265
6.12.2	Applicability of Data Messages .....	266
6.12.3	Applicability of Extended Messages .....	267
6.12.4	Applicability of Extended Control Messages .....	269
6.12.5	Applicability of Structured VDM Commands .....	269
6.12.6	Applicability of Reset Signaling .....	270
6.12.7	Applicability of Fast Role Swap signal .....	270
6.13	Value Parameters .....	272
7.	Power Supply .....	272
7.1	Source Requirements .....	272
7.1.1	Behavioral Aspects .....	272
7.1.2	Source Bulk Capacitance .....	272
7.1.3	Types of Sources .....	273
7.1.4	Source Transitions .....	273
7.1.4.1	Fixed Supply .....	273
7.1.4.1.1	Fixed Supply Positive Voltage Transitions .....	273
7.1.4.1.2	Fixed Supply Negative Voltage Transitions .....	274
7.1.4.2	SPR Programmable Power Supply (PPS) .....	275
7.1.4.2.1	SPR Programmable Power Supply Voltage Transitions .....	275
7.1.4.2.2	SPR Programmable Power Supply Current Limit .....	277
7.1.4.2.3	SPR PPS Constant Power Mode .....	280
7.1.4.3	EPR Adjustable Voltage Supply (AVS) .....	281
7.1.4.3.1	EPR Adjustable Voltage Supply Voltage Transitions .....	281
7.1.4.3.2	EPR Adjustable Voltage Supply Current .....	283
7.1.5	Response to Hard Resets .....	283
7.1.6	Changing the Output Power Capability .....	284
7.1.7	Robust Source Operation .....	284
7.1.7.1	Output Over Current Protection .....	284
7.1.7.2	Over Temperature Protection .....	285
7.1.7.3	vSafe5V Externally Applied to Ports Supplying vSafe5V .....	285
7.1.7.4	Detach .....	285
7.1.7.5	Output Voltage Limit .....	285
7.1.8	Output Voltage Tolerance and Range .....	286
7.1.8.1	Programmable Power Supply Output Voltage Tolerance and Range .....	286

7.1.8.2	Adjustable Voltage Supply Output Voltage tolerance and Range .....	287
7.1.9	Charging and Discharging the Bulk Capacitance on $V_{BUS}$ .....	287
7.1.10	Swap Standby for Sources .....	287
7.1.11	Source Peak Current Operation .....	287
7.1.12	Source Capabilities Extended Parameters .....	289
7.1.12.1	Voltage Regulation Field .....	289
7.1.12.1.1	Load Step Slew Rate .....	289
7.1.12.1.2	Load Step Magnitude .....	289
7.1.12.2	Holdup Time Field .....	289
7.1.12.3	Compliance Field .....	290
7.1.12.4	Peak Current .....	290
7.1.12.5	Source Inputs .....	290
7.1.12.6	Batteries .....	291
7.1.13	Fast Role Swap .....	291
7.1.14	Non-application of $V_{BUS}$ Slew Rate Limits .....	292
7.1.15	VCONN Power Cycle .....	293
7.1.15.1	UFP VCONN Power Cycle .....	293
7.1.15.2	DFP VCONN Power Cycle .....	293
7.2	Sink Requirements .....	294
7.2.1	Behavioral Aspects .....	294
7.2.2	Sink Bulk Capacitance .....	294
7.2.3	Sink Standby .....	295
7.2.3.1	Programmable Power Supply Sink Standby .....	295
7.2.4	Suspend Power Consumption .....	295
7.2.5	Zero Negotiated Current .....	295
7.2.6	Transient Load Behavior .....	295
7.2.7	Swap Standby for Sinks .....	296
7.2.8	Sink Peak Current Operation .....	296
7.2.9	Robust Sink Operation .....	296
7.2.9.1	Sink Bulk Capacitance Discharge at Detach .....	296
7.2.9.2	Input Over Voltage Protection .....	297
7.2.9.3	Over Temperature Protection .....	297
7.2.9.4	Over Current Protection .....	297
7.2.10	Fast Role Swap .....	298
7.3	Transitions .....	299
7.3.1	Increasing the Current .....	300
7.3.2	Increasing the Voltage .....	302
7.3.3	Increasing the Voltage and Current .....	304
7.3.4	Increasing the Voltage and Decreasing the Current .....	306
7.3.5	Decreasing the Voltage and Increasing the Current .....	308
7.3.6	Decreasing the Current .....	310
7.3.7	Decreasing the Voltage .....	312
7.3.8	Decreasing the Voltage and the Current .....	314
7.3.9	Sink Requested Power Role Swap .....	316
7.3.10	Source Requested Power Role Swap .....	318
7.3.11	GotoMin Current Decrease .....	320
7.3.12	Source Initiated Hard Reset .....	322
7.3.13	Sink Initiated Hard Reset .....	324

7.3.14	No change in Current or Voltage .....	326
7.3.15	Fast Role Swap .....	328
7.3.16	Increasing the Programmable Power Supply (PPS) Voltage .....	330
7.3.17	Decreasing the Programmable Power Supply (PPS) Voltage .....	332
7.3.18	Increasing the Adjustable Voltage Supply (AVS) Voltage .....	334
7.3.19	Decreasing the Adjustable Voltage Supply (AVS) Voltage .....	336
7.3.20	Changing the Source PDO or APDO .....	338
7.3.21	Increasing the Programmable Power Supply Current .....	340
7.3.22	Decreasing the Programmable Power Supply Current .....	342
7.3.23	Same Request Programmable Power Supply .....	344
7.4	Electrical Parameters .....	345
7.4.1	Source Electrical Parameters .....	345
7.4.2	Sink Electrical Parameters .....	351
7.4.3	Common Electrical Parameters .....	352
8.	Device Policy .....	353
8.1	Overview .....	353
8.2	Device Policy Manager .....	353
8.2.1	Capabilities .....	355
8.2.2	System Policy .....	355
8.2.3	Control of Source/Sink .....	355
8.2.4	Cable Detection .....	355
8.2.4.1	Device Policy Manager in a Provider .....	355
8.2.4.2	Device Policy Manager in a Consumer .....	356
8.2.4.3	Device Policy Manager in a Consumer/Provider .....	356
8.2.4.4	Device Policy Manager in a Provider/Consumer .....	356
8.2.5	Managing Power Requirements .....	356
8.2.5.1	Managing the Power Reserve .....	356
8.2.5.2	Power Capability Mismatch .....	357
8.2.5.2.1	Local device handling of mismatch .....	357
8.2.5.2.2	Device Policy Manager Communication with System Policy .....	357
8.2.6	Use of “Unconstrained Power” bit with Batteries and AC supplies .....	358
8.2.6.1	AC Supplies .....	358
8.2.6.2	Battery Supplies .....	359
8.2.7	Interface to the Policy Engine .....	360
8.2.7.1	Device Policy Manager in a Provider .....	360
8.2.7.2	Device Policy Manager in a Consumer .....	360
8.2.7.3	Device Policy Manager in a Dual-Role Power Device .....	360
8.2.7.4	Device Policy Manager in a Dual-Role Power Device Dead Battery handling .....	360
8.3	Policy Engine .....	361
8.3.1	Introduction .....	361
8.3.2	Atomic Message Sequence Diagrams .....	361
8.3.2.1	Introduction .....	361
8.3.2.1.1	Basic Message Exchange .....	361
8.3.2.1.2	Errors in Basic Message flow .....	362
8.3.2.1.3	Interruptible and Non-Interruptible Atomic Message Sequences .....	366
8.3.2.2	Power Negotiation .....	367

8.3.2.2.1	SPR.....	367
8.3.2.2.2	EPR.....	375
8.3.2.3	Soft Reset.....	394
8.3.2.4	Data Reset.....	396
8.3.2.4.1	DFP Initiated Data Reset where the DFP is the VCONN Source.....	396
8.3.2.4.2	DFP Receives Data Reset where the DFP is the VCONN Source.....	398
8.3.2.4.3	DFP Initiated Data Reset where the UFP is the VCONN Source.....	401
8.3.2.4.4	DFP Receives Data Reset where the UFP is the VCONN Source.....	405
8.3.2.5	Hard Reset.....	409
8.3.2.5.1	Source Initiated Hard Reset.....	409
8.3.2.5.2	Sink Initiated Hard Reset.....	412
8.3.2.5.3	Source Initiated Hard Reset – Sink Long Reset.....	415
8.3.2.6	Power Role Swap.....	419
8.3.2.6.1	Source Initiated Power Role Swap without subsequent Power Negotiation.....	419
8.3.2.6.2	Sink Initiated Power Role Swap without subsequent Power Negotiation.....	424
8.3.2.7	Fast Role Swap.....	429
8.3.2.8	Data Role Swap.....	434
8.3.2.8.1	Data Role Swap, Initiated by UFP Operating as Sink.....	434
8.3.2.8.2	Data Role Swap, Initiated by UFP Operating as Source.....	436
8.3.2.8.3	Data Role Swap, Initiated by DFP Operating as Source.....	438
8.3.2.8.4	Data Role Swap, Initiated by DFP Operating as Sink.....	440
8.3.2.9	VCONN Swap.....	442
8.3.2.9.1	Source to Sink VCONN Source Swap.....	442
8.3.2.9.2	Sink to Source VCONN Source Swap.....	445
8.3.2.10	Additional Capabilities, Status and Information.....	448
8.3.2.10.1	Alert.....	448
8.3.2.10.2	Status.....	451
8.3.2.10.3	Source/Sink Capabilities.....	457
8.3.2.10.4	Extended Capabilities.....	465
8.3.2.10.5	Battery Capabilities and Status.....	469
8.3.2.10.6	Manufacturer Information.....	477
8.3.2.10.7	Country Codes.....	487
8.3.2.10.8	Country Information.....	493
8.3.2.11	Security.....	499
8.3.2.11.1	Source requests security exchange with Sink.....	499
8.3.2.11.2	Sink requests security exchange with Source.....	501
8.3.2.11.3	VCONN Source requests security exchange with Cable Plug.....	503
8.3.2.12	Firmware Update.....	505
8.3.2.12.1	Source requests firmware update exchange with Sink.....	505

8.3.2.12.2	Sink requests firmware update exchange with Source .....	507
8.3.2.12.3	VCONN Source requests firmware update exchange with Cable Plug .....	509
8.3.2.13	Structured VDM .....	511
8.3.2.13.1	DFP to UFP Discover Identity .....	511
8.3.2.13.2	Source Port to Cable Plug Discover Identity .....	512
8.3.2.13.3	DFP to Cable Plug Discover Identity .....	515
8.3.2.13.4	DFP to UFP Enter Mode .....	517
8.3.2.13.5	DFP to UFP Exit Mode .....	519
8.3.2.13.6	DFP to Cable Plug Enter Mode .....	521
8.3.2.13.7	DFP to Cable Plug Exit Mode .....	523
8.3.2.13.8	UFP to DFP Attention .....	525
8.3.2.14	Built in Self-Test (BIST) .....	526
8.3.2.14.1	BIST Carrier Mode .....	526
8.3.2.14.2	BIST Test Data .....	527
8.3.2.15	Enter USB .....	531
8.3.2.15.1	UFP Entering USB4™ Mode (Valid) .....	531
8.3.2.15.2	Cable Plug Entering USB4 Mode (Valid) .....	533
8.3.2.15.3	UFP Entering USB4 Mode (Invalid) .....	534
8.3.2.15.4	Cable Plug Entering USB4 Mode (Invalid) .....	536
8.3.2.16	Unstructured Vendor Defined Messages .....	538
8.3.2.16.1	Unstructured VDM .....	538
8.3.2.16.2	Unstructured VDEM .....	540
8.3.3	State Diagrams .....	542
8.3.3.1	Introduction to state diagrams used in Chapter 8 .....	542
8.3.3.2	Policy Engine Source Port State Diagram .....	544
8.3.3.2.1	PE_SRC_Startup State .....	546
8.3.3.2.2	PE_SRC_Discovery State .....	546
8.3.3.2.3	PE_SRC_Send_Capabilities State .....	547
8.3.3.2.4	PE_SRC_Negotiate_Capability State .....	548
8.3.3.2.5	PE_SRC_Transition_Supply State .....	548
8.3.3.2.6	PE_SRC_Ready State .....	548
8.3.3.2.7	PE_SRC_Disabled State .....	549
8.3.3.2.8	PE_SRC_Capability_Response State .....	549
8.3.3.2.9	PE_SRC_Hard_Reset State .....	550
8.3.3.2.10	PE_SRC_Hard_Reset_Received State .....	550
8.3.3.2.11	PE_SRC_Transition_to_default State .....	550
8.3.3.2.12	PE_SRC_Get_Sink_Cap State .....	551
8.3.3.2.13	PE_SRC_Wait_New_Capabilities State .....	551
8.3.3.2.14	PE_SRC_EPR_Keep_Alive State .....	551
8.3.3.2.15	PE_SRC_Give_Source_Cap State .....	551
8.3.3.3	Policy Engine Sink Port State Diagram .....	553
8.3.3.3.1	PE_SNK_Startup State .....	554
8.3.3.3.2	PE_SNK_Discovery State .....	554
8.3.3.3.3	PE_SNK_Wait_for_Capabilities State .....	554
8.3.3.3.4	PE_SNK_Evaluate_Capability State .....	554
8.3.3.3.5	PE_SNK_Select_Capability State .....	555
8.3.3.3.6	PE_SNK_Transition_Sink State .....	555

8.3.3.3.7	PE_SNK_Ready State .....	555
8.3.3.3.8	PE_SNK_Hard_Reset State .....	556
8.3.3.3.9	PE_SNK_Transition_to_default State .....	557
8.3.3.3.10	PE_SNK_Give_Sink_Cap State .....	557
8.3.3.3.11	PE_SNK_EPR_Keep_Alive .....	557
8.3.3.3.12	PE_SNK_Get_Source_Cap State .....	557
8.3.3.4	SOP Soft Reset and Protocol Error State Diagrams .....	558
8.3.3.4.1	Source Port Soft Reset and Protocol Error State Diagram .....	558
8.3.3.4.2	SOP Sink Port Soft Reset and Protocol Error State Diagram .....	560
8.3.3.5	Data Reset State Diagrams .....	561
8.3.3.5.1	DFP Data_Reset Message State Diagrams .....	561
8.3.3.5.2	UFP Data_Reset Message State Diagrams .....	563
8.3.3.6	Not Supported Message State Diagrams .....	565
8.3.3.6.1	Source Port Not Supported Message State Diagram .....	565
8.3.3.6.2	Sink Port Not Supported Message State Diagram .....	567
8.3.3.7	Source Port Ping State Diagram .....	568
8.3.3.7.1	PE_SRC_Ping State .....	568
8.3.3.8	Source Alert State Diagrams .....	568
8.3.3.8.1	Source Port Source Alert State Diagram .....	568
8.3.3.8.2	Sink Port Source Alert State Diagram .....	568
8.3.3.8.3	Sink Port Sink Alert State Diagram .....	569
8.3.3.8.4	Source Port Sink Alert State Diagram .....	569
8.3.3.9	Source Capabilities Extended State Diagrams .....	570
8.3.3.9.1	Sink Port Get Source Capabilities Extended State Diagram .....	570
8.3.3.9.2	Source Give Source Capabilities Extended State Diagram .....	570
8.3.3.10	Status State Diagrams .....	571
8.3.3.10.1	Sink Port Get Source Status State Diagram .....	571
8.3.3.10.2	Source Give Source Status State Diagram .....	571
8.3.3.10.3	Source Port Get Sink Status State Diagram .....	572
8.3.3.10.4	Sink Give Sink Status State Diagram .....	572
8.3.3.10.5	Sink Port Get Source PPS Status State Diagram .....	572
8.3.3.10.6	Source Give Source PPS Status State Diagram .....	573
8.3.3.11	Battery Capabilities State Diagrams .....	573
8.3.3.11.1	Get Battery Capabilities State Diagram .....	573
8.3.3.11.2	Give Battery Capabilities State Diagram .....	574
8.3.3.12	Battery Status State Diagrams .....	574
8.3.3.12.1	Get Battery Status State Diagram .....	574
8.3.3.12.2	Give Battery Status State Diagram .....	575
8.3.3.13	Manufacturer Information State Diagrams .....	575
8.3.3.13.1	Get Manufacturer Information State Diagram .....	575
8.3.3.13.2	Give Manufacturer Information State Diagram .....	576
8.3.3.14	Country Codes and Information State Diagrams .....	577
8.3.3.14.1	Get Country Codes State Diagram .....	577
8.3.3.14.2	Give Country Codes State Diagram .....	577

8.3.3.14.3	Get Country Information State Diagram .....	578
8.3.3.14.4	Give Country Information State Diagram .....	578
8.3.3.15	Enter_USB Message State Diagrams .....	579
8.3.3.15.1	DFP Enter_USB Message State Diagrams .....	579
8.3.3.15.2	UFP or Cable Plug Enter_USB Message State Diagrams .....	579
8.3.3.16	Security State Diagrams.....	580
8.3.3.16.1	Send Security Request State Diagram .....	580
8.3.3.16.2	Send Security Response State Diagram.....	580
8.3.3.16.3	Security Response Received State Diagram .....	581
8.3.3.17	Firmware Update State Diagrams.....	581
8.3.3.17.1	Send Firmware Update Request State Diagram .....	581
8.3.3.17.2	Send Firmware Update Response State Diagram.....	581
8.3.3.17.3	Firmware Update Response Received State Diagram.....	582
8.3.3.18	Dual-Role Port State Diagrams .....	582
8.3.3.18.1	DFP to UFP Data Role Swap State Diagram .....	583
8.3.3.18.2	UFP to DFP Data Role Swap State Diagram .....	585
8.3.3.18.3	Policy Engine in Source to Sink Power Role Swap State Diagram .....	587
8.3.3.18.4	Policy Engine in Sink to Source Power Role Swap State Diagram .....	589
8.3.3.18.5	Policy Engine in Source to Sink Fast Role Swap State Diagram.....	592
8.3.3.18.6	Policy Engine in Sink to Source Fast Role Swap State Diagram.....	594
8.3.3.18.7	Source Port Get Source Capabilities State Diagram.....	597
8.3.3.18.8	Dual-Role (Source Port) Give Sink Capabilities State Diagram.....	598
8.3.3.18.9	Dual-Role (Sink Port) Get Sink Capabilities State Diagram.....	598
8.3.3.18.10	..... Dual-Role (Sink Port) Give Source Capabilities State Diagram.....	599
8.3.3.18.11	..... Dual-Role (Source Port) Get Source Capabilities Extended State Diagram .....	599
8.3.3.18.12	..... Dual-Role (Sink Port) Give Source Capabilities Extended State Diagram .....	600
8.3.3.19	VCONN Swap State Diagram .....	600
8.3.3.19.1	PE_VCS_Send_Swap State .....	601
8.3.3.19.2	PE_VCS_Evaluate_Swap State .....	602
8.3.3.19.3	PE_VCS_Accept_Swap State .....	602
8.3.3.19.4	PE_VCS_Reject_Swap State .....	602
8.3.3.19.5	PE_VCS_UFP_Wait_for_VCONN State.....	603
8.3.3.19.6	PE_VCS_Turn_Off_VCONN State.....	603
8.3.3.19.7	PE_VCS_Turn_On_VCONN State.....	603
8.3.3.19.8	PE_VCS_Send_PS_Rdy State .....	603
8.3.3.19.9	PE_VCS_Force_VCONN State .....	603
8.3.3.20	Initiator Structured VDM State Diagrams .....	603
8.3.3.20.1	Initiator Structured VDM Discover Identity State Diagram.....	603



8.3.3.20.2	Initiator Structured VDM Discover SVIDs State Diagram.....	605
8.3.3.20.3	Initiator Structured VDM Discover Modes State Diagram.....	606
8.3.3.20.4	Initiator Structured VDM Attention State Diagram.....	607
8.3.3.21	Responder Structured VDM State Diagrams.....	608
8.3.3.21.1	Responder Structured VDM Discover Identity State Diagram.....	608
8.3.3.21.2	Responder Structured VDM Discover SVIDs State Diagram.....	608
8.3.3.21.3	Responder Structured VDM Discover Modes State Diagram.....	609
8.3.3.21.4	Receiving a Structured VDM Attention State Diagram.....	610
8.3.3.22	DFP Structured VDM State Diagrams.....	611
8.3.3.22.1	DFP Structured VDM Mode Entry State Diagram .....	611
8.3.3.22.2	DFP Structured VDM Mode Exit State Diagram.....	612
8.3.3.23	UFP Structured VDM State Diagrams.....	613
8.3.3.23.1	UFP Structured VDM Enter Mode State Diagram .....	614
8.3.3.23.2	UFP Structured VDM Exit Mode State Diagram.....	615
8.3.3.24	Cable Plug Specific State Diagrams.....	616
8.3.3.24.1	Cable Plug Cable Ready State Diagram.....	616
8.3.3.24.2	Soft/Hard/Cable Reset .....	616
8.3.3.24.3	Source Startup Structured VDM Discover Identity of a Cable Plug State Diagram .....	620
8.3.3.24.4	Cable Plug Mode Entry/Exit .....	621
8.3.3.25	EPR Mode State Diagrams.....	624
8.3.3.25.1	Source EPR Mode Entry State Diagram .....	624
8.3.3.25.2	Sink EPR Mode Entry State Diagram .....	626
8.3.3.25.3	Source EPR Mode Exit State Diagram .....	627
8.3.3.25.4	Sink EPR Mode Exit State Diagram .....	628
8.3.3.26	BIST State diagrams.....	628
8.3.3.26.1	BIST Carrier Mode State Diagram.....	628
8.3.3.27	USB Type-C Referenced States .....	629
8.3.3.27.1	ErrorRecovery state .....	629
8.3.3.28	Policy Engine States .....	630
9.	States and Status Reporting .....	636
9.1	Overview .....	636
9.1.1	PDUSB Device and Hub Requirements .....	638
9.1.2	Mapping to USB Device States .....	638
9.1.3	PD Software Stack.....	641
9.1.4	PDUSB Device Enumeration.....	641
9.2	PD Specific Descriptors.....	643
9.2.1	USB Power Delivery Capability Descriptor .....	643
9.2.2	Battery Info Capability Descriptor .....	644
9.2.3	PD Consumer Port Capability Descriptor .....	645
9.2.4	PD Provider Port Capability Descriptor .....	645
9.3	PD Specific Requests and Events .....	646
9.3.1	PD Specific Requests .....	646
9.4	PDUSB Hub and PDUSB Peripheral Device Requests.....	647



9.4.1	GetBatteryStatus .....	647
9.4.2	SetPDFeature .....	648
9.4.2.1	BATTERY_WAKE_MASK Feature Selector .....	648
9.4.2.2	CHARGING_POLICY Feature Selector .....	649
10.	Power Rules .....	650
10.1	Introduction .....	650
10.2	Source Power Rules .....	650
10.2.1	Source Power Rule Considerations .....	650
10.2.2	Normative Voltages and Currents .....	651
10.2.3	Optional Voltages/Currents .....	654
10.2.3.1	Optional Normative Fixed, Variable and Battery Supply .....	654
10.2.3.2	Optional Normative SPR Programmable Power Supply .....	654
10.2.3.2.1	SPR Programmable Power Supply Voltage Ranges .....	655
10.2.3.2.2	Examples of the use of SPR Programmable Power Supplies .....	655
10.2.3.3	Optional Normative Extended Power Range (EPR) .....	656
10.2.3.3.1	EPR Adjustable Voltage Supply (AVS) Voltage Ranges .....	659
10.2.4	Power sharing between ports .....	660
10.3	Sink Power Rules .....	660
10.3.1	Sink Power Rule Considerations .....	660
10.3.2	Normative Sink Rules .....	660
A.	CRC calculation .....	661
A.1	C code example .....	661
A.2	Table showing the full calculation over one Message .....	663
B.	PD Message Sequence Examples .....	664
B.1	External power is supplied downstream .....	664
B.2	External power is supplied upstream .....	667
B.3	Giving back power .....	674
C.	VDM Command Examples .....	684
C.1	Discover Identity Example .....	684
C.1.1	Discover Identity Command request .....	684
C.1.2	Discover Identity Command response – Active Cable. ....	684
C.1.3	Discover Identity Command response – Hub .....	686
C.2	Discover SVIDs Example .....	687
C.2.1	Discover SVIDs Command request .....	687
C.2.2	Discover SVIDs Command response .....	687
C.3	Discover Modes Example .....	689
C.3.1	Discover Modes Command request .....	689
C.3.2	Discover Modes Command response .....	689
C.4	Enter Mode Example .....	691
C.4.1	Enter Mode Command request .....	691
C.4.2	Enter Mode Command response .....	691
C.4.3	Enter Mode Command request with additional VDO .....	692
C.5	Exit Mode Example .....	693
C.5.1	Exit Mode Command request .....	693
C.5.2	Exit Mode Command response .....	693
C.6	Attention Example .....	694

C.6.1	Attention Command request.....	694
C.6.2	Attention Command request with additional VDO.....	694
D.	BMC Receiver Design Examples .....	695
D.1	Finite Difference Scheme .....	695
D.1.1	Sample Circuitry .....	695
D.1.2	Theory .....	695
D.1.3	Data Recovery .....	698
D.1.4	Noise Zone and Detection Zone.....	698
D.2	Subtraction Scheme .....	699
D.2.1	Sample Circuitry .....	699
D.2.2	Output of Each Circuit Block .....	699
D.2.3	Subtractor Output at Power Source and Power Sink .....	700
D.2.4	Noise Zone and Detection Zone.....	701
E.	FRS System Level Example.....	701
E.1	Overview.....	701
E.2	FRS Initial Setup .....	703
E.3	FRS Process .....	705

## List of Tables

Table 1-1 Terms and Abbreviations.....	55
Table 2-1 Fixed Voltage Power Ranges .....	82
Table 2-2 PPS Voltage Power Ranges .....	83
Table 2-3 EPR Adjustable Voltage Supply Voltage Ranges .....	83
Table 5-1 4b5b Symbol Encoding Table .....	86
Table 5-2 Ordered Sets. ....	87
Table 5-3 Validation of Ordered Sets .....	87
Table 5-4 Data Size .....	88
Table 5-5 SOP ordered set. ....	89
Table 5-6 SOP' ordered set. ....	90
Table 5-7 SOP'' ordered set.....	90
Table 5-8 SOP'_Debug ordered set. ....	91
Table 5-9 SOP''_Debug ordered set.....	91
Table 5-10 CRC-32 Mapping.....	92
Table 5-11 Hard Reset ordered set. ....	93
Table 5-12 Cable Reset ordered set. ....	94
Table 5-13 Rp values used for Collision Avoidance.....	95
Table 5-14 BMC Tx Mask Definition, X Values .....	99
Table 5-15 BMC Tx Mask Definition, Y Values .....	100
Table 5-16 BMC Rx Mask Definition.....	104
Table 5-17 BMC Common Normative Requirements.....	106
Table 5-18 BMC Transmitter Normative Requirements .....	106
Table 5-19 BMC Receiver Normative Requirements.....	109
Table 6-1 Message Header .....	114
Table 6-2 Revision Interoperability during an Explicit Contract.....	117
Table 6-3 Extended Message Header .....	118
Table 6-4 Use of Unchunked Message Supported bit .....	120
Table 6-5 Control Message Types.....	124
Table 6-6 Data Message Types.....	133
Table 6-7 Power Data Object .....	134
Table 6-8 Augmented Power Data Object .....	135
Table 6-9 Fixed Supply PDO - Source.....	137
Table 6-10 Fixed Power Source Peak Current Capability .....	139
Table 6-11 Variable Supply (non-Battery) PDO - Source .....	139
Table 6-12 Battery Supply PDO - Source .....	140
Table 6-13 SPR Programmable Power Supply APDO - Source.....	140
Table 6-14 EPR Adjustable Voltage Supply APDO – Source .....	141
Table 6-15 Fixed Supply PDO - Sink.....	141
Table 6-16 Variable Supply (non-Battery) PDO - Sink .....	143
Table 6-17 Battery Supply PDO - Sink .....	143
Table 6-18 Programmable Power Supply APDO - Sink.....	144
Table 6-19 EPR Adjustable Voltage Supply APDO - Sink .....	144

Table 6-20 Fixed and Variable Request Data Object .....	145
Table 6-21 Fixed and Variable Request Data Object with GiveBack Support .....	145
Table 6-22 Battery Request Data Object .....	145
Table 6-23 Battery Request Data Object with GiveBack Support .....	145
Table 6-24 Programmable Request Data Object .....	146
Table 6-25 AVS Request Data Object .....	146
Table 6-26 BIST Data Object .....	150
Table 6-27 Unstructured VDM Header .....	153
Table 6-28 Structured VDM Header .....	154
Table 6-29 Structured VDM Commands .....	155
Table 6-30 SVID Values .....	155
Table 6-31 Commands and Responses .....	157
Table 6-32 ID Header VDO .....	159
Table 6-33 Product Types (UFP) .....	160
Table 6-34 Product Types (Cable Plug/VPD) .....	160
Table 6-35 Product Types (DFP) .....	161
Table 6-36 Cert Stat VDO .....	161
Table 6-37 Product VDO .....	161
Table 6-38 UFP VDO .....	162
Table 6-39 DFP VDO .....	163
Table 6-40 Passive Cable VDO .....	164
Table 6-41 Active Cable VDO 1 .....	166
Table 6-42 Active Cable VDO 2 .....	169
Table 6-43 VPD VDO .....	171
Table 6-44 Discover SVIDs Responder VDO .....	172
Table 6-45 Battery Status Data Object (BSDO) .....	180
Table 6-46 Alert Data Object .....	181
Table 6-47 Country Code Data Object .....	184
Table 6-48 Enter_USB Data Object .....	184
Table 6-49 EPR Mode Data Object (EPRMDO) .....	187
Table 6-50 Source_Info Data Object .....	191
Table 6-51 Revision Data Object .....	192
Table 6-52 Extended Message Types .....	193
Table 6-53 Source Capabilities Extended Data Block (SCEDB) .....	194
Table 6-54 SOP Status Data Block (SDB) .....	198
Table 6-55 SOP'/SOP'' Status Data Block (SDB) .....	202
Table 6-56 Get Battery Cap Data Block (GBCDB) .....	202
Table 6-57 Get Battery Status Data Block (GBSDB) .....	203
Table 6-58 Battery Capability Data Block (BCDB) .....	203
Table 6-59 Get Manufacturer Info Data Block (GMIDB) .....	204
Table 6-60 Manufacturer Info Data Block (MIDB) .....	205
Table 6-61 PPS Status Data Block (PPSSDB) .....	207
Table 6-62 Country Codes Data Block (CCDB) .....	209

Table 6-63 Country Info Data Block (CIDB).....	209
Table 6-64 Sink Capabilities Extended Data Block (SKEDB) .....	210
Table 6-65 Extended Control Data Block (SDB) .....	214
Table 6-66 Extended Control Message Types .....	214
Table 6-67 Time Values .....	229
Table 6-68 Timers.....	230
Table 6-69 Counter parameters .....	233
Table 6-70 Counters .....	234
Table 6-71 Response to an incoming Message (except VDM) .....	235
Table 6-72 Response to an incoming VDM.....	236
Table 6-73 Message discarding .....	238
Table 6-74 Protocol Layer States .....	262
Table 6-75 Applicability of Control Messages .....	265
Table 6-76 Applicability of Data Messages.....	266
Table 6-77 Applicability of Extended Messages .....	267
Table 6-78 Applicability of Extended Control Messages .....	269
Table 6-79 Applicability of Structured VDM Commands.....	269
Table 6-80 Applicability of Reset Signaling .....	270
Table 6-81 Applicability of Fast Role Swap signal .....	271
Table 6-82 Value Parameters .....	272
Table 7-1 Sequence Description for Increasing the Current.....	301
Table 7-2 Sequence Description for Increasing the Voltage .....	303
Table 7-3 Sequence Diagram for Increasing the Voltage and Current .....	305
Table 7-4 Sequence Description for Increasing the Voltage and Decreasing the Current.....	307
Table 7-5 Sequence Description for Decreasing the Voltage and Increasing the Current.....	309
Table 7-6 Sequence Description for Decreasing the Current .....	311
Table 7-7 Sequence Description for Decreasing the Voltage .....	313
Table 7-8 Sequence Description for Decreasing the Voltage and the Current.....	315
Table 7-9 Sequence Description for a Sink Requested Power Role Swap .....	317
Table 7-10 Sequence Description for a Source Requested Power Role Swap .....	319
Table 7-11 Sequence Description for a GotoMin Current Decrease.....	321
Table 7-12 Sequence Description for a Source Initiated Hard Reset .....	323
Table 7-13 Sequence Description for a Sink Initiated Hard Reset.....	325
Table 7-14 Sequence Description for no change in Current or Voltage.....	327
Table 7-15 Sequence Description for Fast Role Swap.....	328
Table 7-16 Sequence Description for Increasing the Programmable Power Supply Voltage .....	330
Table 7-17 Sequence Description for Decreasing the Programmable Power Supply Voltage .....	332
Table 7-18 Sequence Description for Increasing the Adjustable Voltage Supply Voltage.....	334
Table 7-19 Sequence Description for Decreasing the Adjustable Voltage Supply Voltage .....	336
Table 7-20 Sequence Description for Changing the Source PDO or APDO .....	338
Table 7-21 Sequence Description for increasing the Current in PPS mode.....	340

Table 7-22 Sequence Description for decreasing the Current in PPS mode.....	342
Table 7-23 Sequence Description for no change in Current or Voltage in PPS mode.....	344
Table 7-24 Source Electrical Parameters .....	345
Table 7-25 Sink Electrical Parameters .....	351
Table 7-26 Common Source/Sink Electrical Parameters.....	352
Table 8-1 Basic Message Flow .....	362
Table 8-2 Potential issues in Basic Message Flow .....	363
Table 8-3 Basic Message Flow with CRC failure .....	364
Table 8-4 Interruptible and Non-interruptible AMS.....	366
Table 8-5 Steps for a successful Power Negotiation.....	368
Table 8-6 Steps for a GotoMin Negotiation.....	371
Table 8-7 Steps for SPR PPS Keep Alive.....	373
Table 8-8 Steps for Entering EPR Mode (Success) .....	377
Table 8-9 Steps for Entering EPR Mode (Failure due to non-EPR cable).....	380
Table 8-10 Steps for Entering EPR Mode (Failure of VCONN Swap).....	382
Table 8-11 Steps for a successful EPR Power Negotiation.....	385
Table 8-12 Steps for EPR Keep Alive.....	388
Table 8-13 Steps for Exiting EPR Mode (Sink Initiated).....	390
Table 8-14 Steps for Exiting EPR Mode (Source Initiated) .....	392
Table 8-15 Steps for a Soft Reset .....	394
Table 8-16 Steps for a DFP Initiated Data Reset where the DFP is the VCONN Source.....	397
Table 8-17 Steps for a DFP Receiving a Data Reset where the DFP is the VCONN Source.....	399
Table 8-18 Steps for a DFP Initiated Data Reset where the UFP is the VCONN Source.....	403
Table 8-19 Steps for a DFP Receiving a Data Reset where the UFP is the VCONN Source.....	407
Table 8-20 Steps for Source initiated Hard Reset.....	411
Table 8-21 Steps for Sink initiated Hard Reset.....	414
Table 8-22 Steps for Source initiated Hard Reset – Sink long reset .....	416
Table 8-23 Steps for a Successful Source Initiated Power Role Swap Sequence .....	421
Table 8-24 Steps for a Successful Sink Initiated Power Role Swap Sequence .....	426
Table 8-25 Steps for a Successful Fast Role Swap Sequence.....	431
Table 8-26 Steps for Data Role Swap, UFP operating as Sink initiates .....	434
Table 8-27 Steps for Data Role Swap, UFP operating as Source initiates .....	436
Table 8-28 Steps for Data Role Swap, DFP operating as Source initiates .....	438
Table 8-29 Steps for Data Role Swap, DFP operating as Sink initiates .....	440
Table 8-30 Steps for Source to Sink VCONN Source Swap.....	443
Table 8-31 Steps for Sink to Source VCONN Source Swap.....	446
Table 8-32 Steps for Source Alert to Sink .....	449
Table 8-33 Steps for Sink Alert to Source .....	450
Table 8-34 Steps for a Sink getting Source Status Sequence.....	451
Table 8-35 Steps for a Source getting Sink Status Sequence.....	453
Table 8-36 Steps for a Sink getting Source PPS status Sequence .....	455
Table 8-37 Steps for a Sink getting Source Capabilities Sequence .....	457

Table 8-38 Steps for a Dual-Role Source getting Dual-Role Sink's capabilities as a Source Sequence .....	459
Table 8-39 Steps for a Source getting Sink Capabilities Sequence .....	461
Table 8-40 Steps for a Dual-Role Sink getting Dual-Role Source capabilities as a Sink Sequence .....	463
Table 8-41 Steps for a Sink getting Source extended capabilities Sequence .....	465
Table 8-42 Steps for a Dual-Role Source getting Dual-Role Sink extended capabilities Sequence .....	467
Table 8-43 Steps for a Sink getting Source Battery capabilities Sequence .....	469
Table 8-44 Steps for a Source getting Sink Battery capabilities Sequence .....	471
Table 8-45 Steps for a Sink getting Source Battery status Sequence .....	473
Table 8-46 Steps for a Source getting Sink Battery status Sequence .....	475
Table 8-47 Steps for a Source getting Sink's Port Manufacturer Information Sequence.....	477
Table 8-48 Steps for a Source getting Sink's Port Manufacturer Information Sequence.....	479
Table 8-49 Steps for a Source getting Sink's Battery Manufacturer Information Sequence .....	481
Table 8-50 Steps for a Source getting Sink's Battery Manufacturer Information Sequence .....	483
Table 8-51 Steps for a VCONN Source getting Sink's Port Manufacturer Information Sequence .....	485
Table 8-52 Steps for a Source getting Country Codes Sequence .....	487
Table 8-53 Steps for a Source getting Sink's Country Codes Sequence .....	489
Table 8-54 Steps for a VCONN Source getting Sink's Country Codes Sequence.....	491
Table 8-55 Steps for a Source getting Country Information Sequence .....	493
Table 8-56 Steps for a Source getting Sink's Country Information Sequence .....	495
Table 8-57 Steps for a VCONN Source getting Sink's Country Information Sequence .....	497
Table 8-58 Steps for a Source requesting a security exchange with a Sink Sequence.....	499
Table 8-59 Steps for a Sink requesting a security exchange with a Source Sequence.....	501
Table 8-60 Steps for a VCONN Source requesting a security exchange with a Cable Plug Sequence .....	503
Table 8-61 Steps for a Source requesting a firmware update exchange with a Sink Sequence .....	505
Table 8-62 Steps for a Sink requesting a firmware update exchange with a Source Sequence .....	507
Table 8-63 Steps for a VCONN Source requesting a firmware update exchange with a Cable Plug Sequence .....	509
Table 8-64 Steps for DFP to UFP Discover Identity .....	511
Table 8-65 Steps for Source Port to Cable Plug Discover Identity .....	513
Table 8-66 Steps for DFP to Cable Plug Discover Identity.....	515
Table 8-67 Steps for DFP to UFP Enter Mode.....	517
Table 8-68 Steps for DFP to UFP Exit Mode .....	519
Table 8-69 Steps for DFP to Cable Plug Enter Mode.....	521
Table 8-70 Steps for DFP to Cable Plug Exit Mode .....	523
Table 8-71 Steps for UFP to DFP Attention.....	525
Table 8-72 Steps for BIST Carrier Mode Test.....	527
Table 8-73 Steps for BIST Test Data Test.....	529



Table 8-74 Steps for UFP USB4 Mode Entry (Valid).....	531
Table 8-75 Steps for Cable Plug USB4 Mode Entry (Valid) .....	533
Table 8-76 Steps for UFP USB4 Mode Entry (Invalid) .....	535
Table 8-77 Steps for Cable Plug USB4 Mode Entry (Invalid) .....	537
Table 8-78 Steps for Unstructured VDM Message Sequence .....	539
Table 8-79 Steps for Unstructured VDEM Message Sequence .....	541
Table 8-80 Policy Engine States .....	630
Table 9-1 USB Power Delivery Type Codes .....	643
Table 9-2 USB Power Delivery Capability Descriptor .....	643
Table 9-3 Battery Info Capability Descriptor .....	644
Table 9-4 PD Consumer Port Descriptor .....	645
Table 9-5 PD Provider Port Descriptor .....	646
Table 9-6 PD Requests .....	646
Table 9-7 PD Request Codes.....	646
Table 9-8 PD Feature Selectors .....	647
Table 9-9 Battery Status Structure .....	647
Table 9-10 Battery Wake Mask .....	649
Table 9-11 Charging Policy Encoding .....	649
Table 10-1 Considerations for Sources .....	650
Table 10-2 SPR Normative Voltages and Minimum Currents .....	651
Table 10-3 Fixed Supply PDO – Source 5V.....	653
Table 10-4 Fixed Supply PDO – Source 9V.....	653
Table 10-5 Fixed Supply PDO – Source 15V.....	653
Table 10-6 Fixed Supply PDO – Source 20V.....	653
Table 10-7 SPR Programmable Power Supply PDOs and APDOs based on the PDP .....	654
Table 10-8 SPR Programmable Power Supply Voltage Ranges.....	655
Table 10-9 EPR Source Capabilities based in the Port's PDP .....	657
Table 10-10 EPR Source Capabilities based on a Shared Port's Equivalent PDP .....	658
Table 10-11 EPR Source Equivalent PDP Examples .....	659
Table 10-12 EPR Adjustable Voltage Supply (AVS) Voltage Ranges .....	660
Table B-1 External power is supplied downstream .....	665
Table B-2 External power is supplied upstream.....	668
Table B-3 Giving back power. ....	674
Table C-1 Discover Identity Command request from Initiator Example. ....	684
Table C-2 Discover Identity Command response from Active Cable Responder Example .....	685
Table C-3 Discover Identity Command response from Hub Responder Example .....	686
Table C-4 Discover SVIDs Command request from Initiator Example. ....	687
Table C-5 Discover SVIDs Command response from Responder Example. ....	687
Table C-6 Discover Modes Command request from Initiator Example. ....	689
Table C-7 Discover Modes Command response from Responder Example.....	689
Table C-8 Enter Mode Command request from Initiator Example. ....	691
Table C-9 Enter Mode Command response from Responder Example.....	691



Table C-10 Enter Mode Command request from Initiator Example. ....	692
Table C-11 Exit Mode Command request from Initiator Example. ....	693
Table C-12 Exit Mode Command response from Responder Example. ....	693
Table C-13 Attention Command request from Initiator Example.....	694
Table C-14 Attention Command request from Initiator with additional VDO Example .....	695
Table E-1: Sequence Table for setup of a Fast Role Swap (Hub connected to Power Adapter first).....	703
Table E-2 Sequence Table for setup of a Fast Role Swap (Hub connected to Notebook before Power Adapter) .....	704
Table E-3 Sequence Table for slow Vbus discharge (it discharges after FR_Swap message is sent).....	706
Table E-4 Vbus discharges quickly after adapter disconnected. ....	708

## List of Figures

Figure 2-1 Logical Structure of USB Power Delivery Capable Devices .....	66
Figure 2-2 Example SOP' Communication between VCONN Source and Cable Plug(s) .....	68
Figure 2-3 USB Power Delivery Communications Stack .....	75
Figure 2-4 USB Power Delivery Communication Over USB .....	76
Figure 2-5 High Level Architecture View .....	77
Figure 2-6 Example of a Normal EPR Mode Operational Flow .....	82
Figure 5-1 Interpretation of ordered sets .....	87
Figure 5-2 Transmit Order for Various Sizes of Data .....	88
Figure 5-3 USB Power Delivery Packet Format .....	89
Figure 5-4 CRC 32 generation .....	92
Figure 5-5 Line format of Hard Reset .....	94
Figure 5-6 Line format of Cable Reset .....	94
Figure 5-7 BMC Example .....	95
Figure 5-8 BMC Transmitter Block Diagram .....	96
Figure 5-9 BMC Receiver Block Diagram .....	96
Figure 5-10 BMC Encoded Start of Preamble .....	96
Figure 5-11 Transmitting or Receiving BMC Encoded Frame Terminated by Zero with High-to-Low Last Transition .....	97
Figure 5-12 Transmitting or Receiving BMC Encoded Frame Terminated by One with High-to-Low Last Transition .....	97
Figure 5-13 Transmitting or Receiving BMC Encoded Frame Terminated by Zero with Low to High Last Transition .....	98
Figure 5-14 Transmitting or Receiving BMC Encoded Frame Terminated by One with Low to High Last Transition .....	98
Figure 5-15 BMC Tx 'ONE' Mask .....	99
Figure 5-16 BMC Tx 'ZERO' Mask .....	99
Figure 5-17 BMC Rx 'ONE' Mask when Sourcing Power .....	101
Figure 5-18 BMC Rx 'ZERO' Mask when Sourcing Power .....	102
Figure 5-19 BMC Rx 'ONE' Mask when Power neutral .....	102
Figure 5-20 BMC Rx 'ZERO' Mask when Power neutral .....	103
Figure 5-21 BMC Rx 'ONE' Mask when Sinking Power .....	103
Figure 5-22 BMC Rx 'ZERO' Mask when Sinking Power .....	104
Figure 5-23 Transmitter Load Model for BMC Tx from a Source .....	105
Figure 5-24 Transmitter Load Model for BMC Tx from a Sink .....	105
Figure 5-25 Transmitter diagram illustrating zDriver .....	107
Figure 5-26 Inter-Frame Gap Timings .....	108
Figure 5-27 Example Multi-Drop Configuration showing two DRPs .....	110
Figure 5-28 Example Multi-Drop Configuration showing a DFP and UFP .....	110
Figure 5-29 Test Data Frame .....	112
Figure 6-1 USB Power Delivery Packet Format including Control Message Payload .....	113
Figure 6-2 USB Power Delivery Packet Format including Data Message Payload .....	113
Figure 6-3 USB Power Delivery Packet Format including an Extended Message Header and Payload .....	114

Figure 6-4 Example Security_Request sequence Unchunked (Chunked bit = 0) .....	120
Figure 6-5 Example byte transmission for Security_Request Message of Data Size 7 (Chunked bit is set to 0) .....	120
Figure 6-6 Example byte transmission for Security_Response Message of Data Size 7 (Chunked bit is set to 0) .....	121
Figure 6-7 Example Security_Request sequence Chunked (Chunked bit = 1) .....	122
Figure 6-8 Example Security_Request Message of Data Size 7 (Chunked bit set to 1) .....	122
Figure 6-9 Example Chunk 0 of Security_Response Message of Data Size 30 (Chunked bit set to 1) .....	123
Figure 6-10 Example byte transmission for a Security_Response Message Chunk request (Chunked bit is set to 1) .....	123
Figure 6-11 Example Chunk 1 of Security_Response Message of Data Size 30 (Chunked bit set to 1) .....	124
Figure 6-12 Example Capabilities Message with 2 Power Data Objects .....	134
Figure 6-13 BIST Message .....	149
Figure 6-14 Vendor Defined Message .....	152
Figure 6-15 Discover Identity Command response .....	158
Figure 6-16 Discover Identity Command response for a DRD .....	158
Figure 6-17 Example Discover SVIDs response with 3 SVIDs .....	173
Figure 6-18 Example Discover SVIDs response with 4 SVIDs .....	173
Figure 6-19 Example Discover SVIDs response with 12 SVIDs followed by an empty response .....	173
Figure 6-20 Example Discover Modes response for a given SVID with 3 Modes .....	174
Figure 6-21 Successful Enter Mode sequence .....	175
Figure 6-22 Enter Mode sequence Interrupted by Source Capabilities and then Re-run .....	175
Figure 6-23 Unsuccessful Enter Mode sequence due to NAK .....	176
Figure 6-24 Exit Mode sequence .....	177
Figure 6-25 Attention Command request/response sequence .....	177
Figure 6-26 Command request/response sequence .....	178
Figure 6-27 Enter/Exit Mode Process .....	179
Figure 6-28 Battery_Status Message .....	180
Figure 6-29 Alert Message .....	181
Figure 6-30 Get_Country_Info Message .....	184
Figure 6-31 Enter_USB Message .....	184
Figure 6-32 EPR_Request Message .....	186
Figure 6-33 EPR Mode DO Message .....	187
Figure 6-34 Illustration of process to enter EPR Mode .....	188
Figure 6-35 Source_Info Message .....	191
Figure 6-36 Revision Message Data Object .....	192
Figure 6-37 Source_Capabilities_Extended Message .....	194
Figure 6-38 SOP Status Message .....	198
Figure 6-39 SOP'/SOP'' Status Message .....	202
Figure 6-40 Get_Battery_Cap Message .....	202
Figure 6-41 Get_Battery_Status Message .....	203
Figure 6-42 Battery_Capabilities Message .....	203

Figure 6-43 Get_Manufacturer_Info Message .....	204
Figure 6-44 Manufacturer_Info Message .....	205
Figure 6-45 Security_Request Message .....	206
Figure 6-46 Security_Response Message .....	206
Figure 6-47 Firmware_Update_Request Message .....	207
Figure 6-48 Firmware_Update_Response Message .....	207
Figure 6-49 PPS_Status Message .....	207
Figure 6-50 Country_Codes Message .....	209
Figure 6-51 Country_Info Message .....	209
Figure 6-52 Sink_Capabilities_Extended Message .....	210
Figure 6-53 Extended_Control Message .....	214
Figure 6-54 Mapping SPR Capabilities to EPR Capabilities .....	215
Figure 6-55 Vendor_Defined_Extended Message .....	217
Figure 6-56 Outline of States .....	239
Figure 6-57 References to states .....	239
Figure 6-58 Chunking architecture Showing Message and Control Flow .....	240
Figure 6-59 Chunked Rx State Diagram .....	242
Figure 6-60 Chunked Tx State Diagram .....	245
Figure 6-61 Chunked Message Router State Diagram .....	249
Figure 6-62 Common Protocol Layer Message Transmission State Diagram .....	251
Figure 6-63 Source Protocol Layer Message Transmission State Diagram .....	254
Figure 6-64 Sink Protocol Layer Message Transmission State Diagram .....	255
Figure 6-65 Protocol layer Message reception .....	257
Figure 6-66 Hard/Cable Reset .....	259
Figure 7-1 Placement of Source Bulk Capacitance .....	273
Figure 7-2 Transition Envelope for Positive Voltage Transitions .....	274
Figure 7-3 Transition Envelope for Negative Voltage Transitions .....	275
Figure 7-4 PPS Positive Voltage Transitions .....	276
Figure 7-5 PPS Negative Voltage Transitions .....	277
Figure 7-6 Expected PPS Ripple Relative to an LSB .....	277
Figure 7-7 SPR PPS Programmable Voltage and Current Limit .....	279
Figure 7-8 iPpsCLOperatingDetail .....	280
Figure 7-9 SPR PPS Programmable Voltage and Current Limit .....	281
Figure 7-10 AVS Positive Voltage Transitions .....	282
Figure 7-11 AVS Negative Voltage Transitions .....	282
Figure 7-12 Expected AVS Ripple Relative to an LSB .....	283
Figure 7-13 Source $V_{BUS}$ and $V_{CONN}$ Response to Hard Reset .....	284
Figure 7-14 Application of $v_{SrcNew}$ and $v_{SrcValid}$ limits after $t_{SrcReady}$ .....	286
Figure 7-15 Source Peak Current Overload .....	288
Figure 7-16 Holdup Time Measurement .....	290
Figure 7-17 $V_{BUS}$ Power during Fast Role Swap .....	291
Figure 7-18 $V_{BUS}$ detection and timing during Fast Role Swap, initial $V_{BUS}$ (at new source) > $v_{Safe5V}$ (min). .....	292

Figure 7-19 $V_{BUS}$ detection and timing during Fast Role Swap, initial $V_{BUS}$ (at new source) < $vSafe5V$ (min).	292
Figure 7-20 Data Reset UFP VCONN Power Cycle	293
Figure 7-21 Data Reset DFP VCONN Power Cycle	294
Figure 7-22 Placement of Sink Bulk Capacitance	295
Figure 7-23 Transition Diagram for Increasing the Current	300
Figure 7-24 Transition Diagram for Increasing the Voltage	302
Figure 7-25 Transition Diagram for Increasing the Voltage and Current	304
Figure 7-26 Transition Diagram for Increasing the Voltage and Decreasing the Current	306
Figure 7-27 Transition Diagram for Decreasing the Voltage and Increasing the Current	308
Figure 7-28 Transition Diagram for Decreasing the Current	310
Figure 7-29 Transition Diagram for Decreasing the Voltage	312
Figure 7-30 Transition Diagram for Decreasing the Voltage and the Current	314
Figure 7-31 Transition Diagram for a Sink Requested Power Role Swap	316
Figure 7-32 Transition Diagram for a Source Requested Power Role Swap	318
Figure 7-33 Transition Diagram for a GotoMin Current Decrease	320
Figure 7-34 Transition Diagram for a Source Initiated Hard Reset	322
Figure 7-35 Transition Diagram for a Sink Initiated Hard Reset	324
Figure 7-36 Transition Diagram for no change in Current or Voltage	326
Figure 7-37 Transition Diagram for Fast Role Swap	328
Figure 7-38 Transition Diagram for Increasing the Programmable Power Supply Voltage	330
Figure 7-39 Transition Diagram for Decreasing the Programmable Power Supply Voltage	332
Figure 7-40 Transition Diagram for Increasing the Programmable Power Supply Voltage	334
Figure 7-41 Transition Diagram for Decreasing the Adjustable Voltage Supply Voltage	336
Figure 7-42 Transition Diagram for Changing the Source PDO or APDO	338
Figure 7-43 Transition Diagram for increasing the Current in PPS mode	340
Figure 7-44 Transition Diagram for decreasing the Current in PPS mode	342
Figure 7-45 Transition Diagram for no change in Current or Voltage in PPS mode	344
Figure 8-1 Example of daisy chained displays	359
Figure 8-2 Basic Message Exchange (Successful)	362
Figure 8-3 Basic Message flow indicating possible errors	363
Figure 8-4 Basic Message Flow with Bad CRC followed by a Retry	364
Figure 8-5 Successful Fixed, Variable or Battery SPR Power Negotiation	368
Figure 8-6 Successful GotoMin operation	371
Figure 8-7 SPR PPS Keep Alive	373
Figure 8-8 Entering EPR Mode (Success)	376
Figure 8-9 Entering EPR Mode (Failure due to non-EPR cable)	379
Figure 8-10 Entering EPR Mode (Failure of VCONN Swap)	382
Figure 8-11 Successful Fixed EPR Power Negotiation	385
Figure 8-12 EPR Keep Alive	388
Figure 8-13 Exiting EPR Mode (Sink Initiated)	390

Figure 8-14 Exiting EPR Mode (Source Initiated) .....	392
Figure 8-15 Soft Reset.....	394
Figure 8-16 DFP Initiated Data Reset where the DFP is the VCONN Source.....	396
Figure 8-17 DFP Receives Data Reset where the DFP is the VCONN Source.....	399
Figure 8-18 DFP Initiated Data Reset where the UFP is the Vconn Source .....	402
Figure 8-19 DFP Receives a Data Reset where the UFP is the VCONN Source .....	406
Figure 8-20 Source initiated Hard Reset .....	410
Figure 8-21 Sink Initiated Hard Reset .....	413
Figure 8-22 Source initiated reset - Sink long reset.....	416
Figure 8-23 Successful Power Role Swap Sequence Initiated by the Source .....	420
Figure 8-24 Successful Power Role Swap Sequence Initiated by the Sink.....	425
Figure 8-25 Successful Fast Role Swap Sequence .....	430
Figure 8-26 Data Role Swap, UFP operating as Sink initiates .....	434
Figure 8-27 Data Role Swap, UFP operating as Source initiates .....	436
Figure 8-28 Data Role Swap, DFP operating as Source initiates .....	438
Figure 8-29 Data Role Swap, DFP operating as Sink initiates .....	440
Figure 8-30 Source to Sink VCONN Source Swap.....	442
Figure 8-31 Sink to Source VCONN Source Swap.....	445
Figure 8-32 Source Alert to Sink .....	448
Figure 8-33 Sink Alert to Source .....	450
Figure 8-34 Sink Gets Source Status .....	451
Figure 8-35 Source Gets Sink Status .....	453
Figure 8-36 Sink Gets Source PPS Status .....	455
Figure 8-37 Sink Gets Source's Capabilities .....	457
Figure 8-38 Dual-Role Source Gets Dual-Role Sink's Capabilities as a Source .....	459
Figure 8-39 Source Gets Sink's Capabilities .....	461
Figure 8-40 Dual-Role Sink Gets Dual-Role Source's Capabilities as a Sink .....	463
Figure 8-41 Sink Gets Source's Extended Capabilities.....	465
Figure 8-42 Dual-Role Source Gets Dual-Role Sink's Extended Capabilities .....	467
Figure 8-43 Sink Gets Source's Battery Capabilities .....	469
Figure 8-44 Source Gets Sink's Battery Capabilities .....	471
Figure 8-45 Sink Gets Source's Battery Status .....	473
Figure 8-46 Source Gets Sink's Battery Status .....	475
Figure 8-47 Source Gets Sink's Port Manufacturer Information .....	477
Figure 8-48 Sink Gets Source's Port Manufacturer Information .....	479
Figure 8-49 Source Gets Sink's Battery Manufacturer Information .....	481
Figure 8-50 Sink Gets Source's Battery Manufacturer Information .....	483
Figure 8-51 VCONN Source Gets Cable Plug's Manufacturer Information .....	485
Figure 8-52 Source Gets Sink's Country Codes .....	487
Figure 8-53 Sink Gets Source's Country Codes .....	489
Figure 8-54 VCONN Source Gets Cable Plug's Country Codes .....	491
Figure 8-55 Source Gets Sink's Country Information .....	493
Figure 8-56 Sink Gets Source's Country Information .....	495

Figure 8-57 VCONN Source Gets Cable Plug's Country Information .....	497
Figure 8-58 Source requests security exchange with Sink.....	499
Figure 8-59 Sink requests security exchange with Source.....	501
Figure 8-60 VCONN Source requests security exchange with Cable Plug .....	503
Figure 8-61 Source requests firmware update exchange with Sink .....	505
Figure 8-62 Sink requests firmware update exchange with Source .....	507
Figure 8-63 VCONN Source requests firmware update exchange with Cable Plug .....	509
Figure 8-64 DFP to UFP Discover Identity.....	511
Figure 8-65 Source Port to Cable Plug Discover Identity .....	513
Figure 8-66 DFP to Cable Plug Discover Identity .....	515
Figure 8-67 DFP to UFP Enter Mode.....	517
Figure 8-68 DFP to UFP Exit Mode .....	519
Figure 8-69 DFP to Cable Plug Enter Mode .....	521
Figure 8-70 DFP to Cable Plug Exit Mode .....	523
Figure 8-71 UFP to DFP Attention.....	525
Figure 8-72 BIST Carrier Mode Test .....	526
Figure 8-73 BIST Test Data Test.....	528
Figure 8-74 UFP Entering USB4 Mode (Valid).....	531
Figure 8-75 Cable Plug Entering USB4 Mode (Valid) .....	533
Figure 8-76 UFP Entering USB4 Mode (Invalid) .....	535
Figure 8-77 Cable Plug Entering USB4 Mode (Invalid) .....	537
Figure 8-78 Unstructured VDM Message Sequence .....	539
Figure 8-79 Unstructured VDEM Message Sequence .....	541
Figure 8-80 Outline of States .....	542
Figure 8-81 References to states .....	543
Figure 8-82 Example of state reference with conditions .....	543
Figure 8-83 Example of state reference with the same entry and exit.....	543
Figure 8-84 Source Port Policy Engine State Diagram .....	545
Figure 8-85 Sink Port State Diagram.....	553
Figure 8-86 Source Port Soft Reset and Protocol Error State Diagram .....	558
Figure 8-87 Sink Port Soft Reset and Protocol Error Diagram .....	560
Figure 8-88 DFP Data_Reset Message State Diagram.....	562
Figure 8-89 UFP Data_Reset Message State Diagram.....	564
Figure 8-90 Source Port Not Supported Message State Diagram .....	566
Figure 8-91 Sink Port Not Supported Message State Diagram .....	567
Figure 8-92 Source Port Ping State Diagram.....	568
Figure 8-93 Source Port Source Alert State Diagram .....	568
Figure 8-94 Sink Port Source Alert State Diagram .....	568
Figure 8-95 Sink Port Sink Alert State Diagram.....	569
Figure 8-96 Source Port Sink Alert State Diagram .....	569
Figure 8-97 Sink Port Get Source Capabilities Extended State Diagram .....	570
Figure 8-98 Source Give Source Capabilities Extended State Diagram .....	570
Figure 8-99 Sink Port Get Source Status State Diagram .....	571



Figure 8-100 Source Give Source Status State Diagram .....	571
Figure 8-101 Source Port Get Sink Status State Diagram .....	572
Figure 8-102 Sink Give Sink Status State Diagram .....	572
Figure 8-103 Sink Port Get Source PPS Status State Diagram.....	573
Figure 8-104 Source Give Source PPS Status State Diagram .....	573
Figure 8-105 Get Battery Capabilities State Diagram .....	574
Figure 8-106 Give Battery Capabilities State Diagram.....	574
Figure 8-107 Get Battery Status State Diagram .....	575
Figure 8-108 Give Battery Status State Diagram.....	575
Figure 8-109 Get Manufacturer Information State Diagram .....	576
Figure 8-110 Give Manufacturer Information State Diagram.....	576
Figure 8-111 Get Country Codes State Diagram .....	577
Figure 8-112 Give Country Codes State Diagram.....	577
Figure 8-113 Get Country Information State Diagram.....	578
Figure 8-114 Give Country Information State Diagram .....	578
Figure 8-115 DFP Enter_USB Message State Diagram .....	579
Figure 8-116 UFP Enter_USB Message State Diagram .....	579
Figure 8-117 Send security request State Diagram .....	580
Figure 8-118 Send security response State Diagram.....	580
Figure 8-119 Security response received State Diagram .....	581
Figure 8-120 Send firmware update request State Diagram .....	581
Figure 8-121 Send firmware update response State Diagram.....	582
Figure 8-122 Firmware update response received State Diagram.....	582
Figure 8-123: DFP to UFP Data Role Swap State Diagram .....	583
Figure 8-124: UFP to DFP Data Role Swap State Diagram .....	585
Figure 8-125: Dual-Role Port in Source to Sink Power Role Swap State Diagram .....	587
Figure 8-126: Dual-role Port in Sink to Source Power Role Swap State Diagram.....	590
Figure 8-127: Dual-Role Port in Source to Sink Fast Role Swap State Diagram .....	593
Figure 8-128: Dual-role Port in Sink to Source Fast Role Swap State Diagram .....	595
Figure 8-129 Dual-Role (Source) Get Source Capabilities diagram .....	597
Figure 8-130 Dual-Role (Source) Give Sink Capabilities diagram.....	598
Figure 8-131 Dual-Role (Sink) Get Sink Capabilities State Diagram .....	598
Figure 8-132 Dual-Role (Sink) Give Source Capabilities State Diagram .....	599
Figure 8-133 Dual-Role (Source) Get Source Capabilities Extended State Diagram .....	600
Figure 8-134 Dual-Role (Source) Give Sink Capabilities diagram.....	600
Figure 8-135 VCONN Swap State Diagram .....	601
Figure 8-136 Initiator to Port VDM Discover Identity State Diagram .....	604
Figure 8-137 Initiator VDM Discover SVIDs State Diagram .....	605
Figure 8-138 Initiator VDM Discover Modes State Diagram.....	606
Figure 8-139 Initiator VDM Attention State Diagram.....	607
Figure 8-140 Responder Structured VDM Discover Identity State Diagram.....	608
Figure 8-141 Responder Structured VDM Discover SVIDs State Diagram .....	609
Figure 8-142 Responder Structured VDM Discover Modes State Diagram.....	610



Figure 8-143 Receiving a Structured VDM Attention State Diagram .....	611
Figure 8-144 DFP VDM Mode Entry State Diagram .....	611
Figure 8-145 DFP VDM Mode Exit State Diagram .....	613
Figure 8-146 UFP Structured VDM Enter Mode State Diagram .....	614
Figure 8-147 UFP Structured VDM Exit Mode State Diagram .....	615
Figure 8-148 Cable Ready VDM State Diagram .....	616
Figure 8-149 Cable Plug Soft Reset State Diagram .....	616
Figure 8-150 Cable Plug Hard Reset State Diagram .....	617
Figure 8-151 DFP/VCONN Source Soft Reset or Cable Reset of a Cable Plug or VPD State Diagram .....	618
Figure 8-152 UFP/VCONN Source Soft Reset of a Cable Plug or VPD State Diagram .....	619
Figure 8-153 Source Startup Structured VDM Discover Identity State Diagram .....	620
Figure 8-154 Cable Plug Structured VDM Enter Mode State Diagram .....	622
Figure 8-155 Cable Plug Structured VDM Exit Mode State Diagram .....	623
Figure 8-156 Source EPR Mode Entry State Diagram .....	624
Figure 8-157 Sink EPR Mode Entry State Diagram .....	626
Figure 8-158 Source EPR Mode Exit State Diagram .....	627
Figure 8-159 Sink EPR Mode Exit State Diagram .....	628
Figure 8-160 BIST Carrier Mode State Diagram .....	629
Figure 9-1 Example PD Topology .....	637
Figure 9-2 Mapping of PD Topology to USB .....	638
Figure 9-3 USB Attached to USB Powered State Transition .....	639
Figure 9-4 Any USB State to USB Attached State Transition (When operating as a Consumer) .....	640
Figure 9-5 Any USB State to USB Attached State Transition (When operating as a Provider) .....	640
Figure 9-6 Any USB State to USB Attached State Transition (After a USB Type-C Data Role Swap) .....	641
Figure 9-7 Software stack on a PD aware OS .....	641
Figure 9-8 Enumeration of a PDUSB Device .....	642
Figure 10-1 SPR Source Power Rule Illustration .....	652
Figure 10-2 SPR Source Power Rule Example .....	652
Figure 10-3 Valid EPR AVS Operating Region .....	659
Figure B-1 External Power supplied downstream .....	664
Figure B-2 External Power supplied upstream .....	668
Figure B-3 Giving Back Power .....	674
Figure D-1 Circuit Block of BMC Finite Difference Receiver .....	695
Figure D-2 BMC AC and DC noise from VBUS at Power Sink .....	696
Figure D-3 Sample BMC Signals (a) without [USB 2.0] SE0 Noise (b) with [USB 2.0] SE0 Noise .....	697
Figure D-4 Scaled BMC Signal Derivative with 50ns Sampling Rate .....	697
Figure D-5 BMC Signal and Finite Difference Output with Various Time Steps .....	698
Figure D-6 Output of Finite Difference in dash line and Edge Detector in solid line .....	698
Figure D-7 Noise Zone and Detect Zone of BMC Receiver .....	699
Figure D-8 Circuit Block of BMC Subtraction Receiver .....	699

Figure D-9 (a) Output of LPF1 and LPF2 (b) Subtraction of LPF1 and LPF2 Output .....	700
Figure D-10 Output of the BMC LPF1 in blue dash curve and the Subtractor in red solid curve .....	700
Figure E-1 Example FRS Capable System .....	701
Figure E-2 Slow $V_{BUS}$ Discharge.....	702
Figure E-3 Fast $V_{BUS}$ Discharge .....	703
Figure E-4 Sequence Diagram for slow VBUS discharge (it discharges after FR_Swap message is sent).....	706

## 1 Introduction

USB has evolved from a data interface capable of supplying limited power to a primary provider of power with a data interface. Today many devices charge or get their power from USB ports contained in laptops, cars, aircraft or even wall sockets. USB has become a ubiquitous power socket for many small devices such as cell phones, MP3 players and other hand-held devices. Users need USB to fulfill their requirements not only in terms of data but also to provide power to, or charge, their devices simply, often without the need to load a driver, in order to carry out “traditional” USB functions.

There are, however, still many devices which either require an additional power connection to the wall, or exceed the USB rated current in order to operate. Increasingly, international regulations require better energy management due to ecological and practical concerns relating to the availability of power. Regulations limit the amount of power available from the wall which has led to a pressing need to optimize power usage. The USB Power Delivery Specification has the potential to minimize waste as it becomes a standard for charging devices that are not satisfied by [\[USBBC 1.2\]](#).

Wider usage of wireless solutions is an attempt to remove data cabling but the need for “tethered” charging remains. In addition, industrial design requirements drive wired connectivity to do much more over the same connector.

USB Power Delivery is designed to enable the maximum functionality of USB by providing more flexible power delivery along with data over a single cable. Its aim is to operate with and build on the existing USB ecosystem; increasing power levels from existing USB standards, for example Battery Charging, enabling new higher power use cases such as USB powered Hard Disk Drives (HDDs) and printers.

With USB Power Delivery the power direction is no longer fixed. This enables the product with the power (Host or Peripheral) to provide the power. For example, a display with a supply from the wall can power, or charge, a laptop. Alternatively, USB power bricks or chargers are able to supply power to laptops and other battery powered devices through their, traditionally power providing, USB ports.

USB Power Delivery enables hubs to become the means to optimize power management across multiple peripherals by allowing each device to take only the power it requires, and to get more power when required for a given application. For example, battery powered devices can get increased charging current and then give it back temporarily when the user's HDD requires spinning up. **Optionally** the hubs can communicate with the PC to enable even more intelligent and flexible management of power either automatically or with some level of user intervention.

USB Power Delivery allows Low Power cases such as headsets to negotiate for only the power they require. This provides a simple solution that enables USB devices to operate at their optimal power levels.

The Power Delivery Specification, in addition to providing mechanisms to negotiate power also can be used as a side-band channel for standard and vendor defined messaging. Power Delivery enables alternative modes of operation by providing the mechanisms to discover, enter and exit Alternate Modes. The specification also enables discovery of cable capabilities such as supported speeds and current levels.

### 1.1 Overview

This specification defines how USB Devices can negotiate for more current and/or higher or lower Voltages over the USB cable (using the USB Type-C® CC wire as the communications channel) than are defined in the [\[USB 2.0\]](#), [\[USB 3.2\]](#), [\[USB Type-C 2.0\]](#) or [\[USBBC 1.2\]](#) specifications. It allows Devices with greater power requirements than can be met with today's specification to get the power they require to operate from  $V_{BUS}$  and negotiate with external power sources (e.g., Wall Warts). In addition, it allows a Source and Sink to swap power roles such that a Device could supply power to the Host. For example, a display could supply power to a notebook to charge its battery.

The USB Power Delivery Specification is guided by the following principles:

- Works seamlessly with legacy USB Devices
- Compatible with existing spec-compliant USB cables

- Minimizes potential damage from non-compliant cables (e.g., ‘Y’ cables etc.)
- Optimized for low-cost implementations.

This specification defines mechanisms to discover, enter and exit Modes defined either by a standard or by a particular vendor. These Modes can be supported either by the Port Partner or by a cable connecting the two Port Partners.

The specification defines mechanisms to discover the capabilities of cables which can communicate using Power Delivery.

This specification adds a mechanism to swap the data roles such that the upstream facing Port becomes the downstream facing Port and vice versa. It also enables a swap of the end supplying VCONN to a powered cable.

To facilitate optimum charging, the specification defines two mechanisms a USB Charger can Advertise for the Device to use:

1. A list of fixed Voltages each with a maximum current. The Device selects a Voltage and current from the list. This is the traditional model used by Devices that use internal electronics to manage the charging of their battery including modifying the Voltage and current actually supplied to the battery. The side-effect of this model is that the charging circuitry generates heat that may be problematic for small form factor devices.
2. A list of programmable Voltage ranges each with a maximum current (PPS). The Device requests a Voltage (in 20mV increments in SPR PPS Mode and in 100mV increments in EPR AVS Mode) that is within the Advertised range and a maximum current. The USB Charger delivers the requested Voltage until the maximum current is reached at which time the USB charger reduces its output Voltage so as not to supply more than the requested maximum current. During the high current portion of the charge cycle, the USB Charger can be directly connected (through an appropriate safety device) to the battery. This model is used by Devices that want to minimize the thermal impact of their internal charging circuitry.

## 1.2 Purpose

The USB Power Delivery specification defines a power delivery system covering all elements of a USB system including: Hosts, Devices, Hubs, Chargers and cable assemblies. This specification describes the architecture, protocols, power supply behavior, connectors and cabling necessary for managing power delivery over USB at up to 100W. This specification is intended to be fully compatible and extend the existing USB infrastructure. It is intended that this specification will allow system OEMs, power supply and peripheral developers adequate flexibility for product versatility and market differentiation without losing backwards compatibility.

USB Power Delivery is designed to operate independently of the existing USB bus defined mechanisms used to negotiate power which are:

- [\[USB 2.0\]](#), [\[USB 3.2\]](#) in band requests for high power interfaces.
- [\[USBBC 1.2\]](#) mechanisms for supplying higher power (not mandated by this specification).
- [\[USB Type-C 2.0\]](#) mechanisms for supplying higher power.

Initial operating conditions remain the USB Default Operation as defined in [\[USB 2.0\]](#), [\[USB 3.2\]](#), [\[USB Type-C 2.0\]](#) or [\[USBBC 1.2\]](#).

- The DFP sources *vSafe5V* over  $V_{BUS}$ .
- The UFP consumes power from  $V_{BUS}$ .

## 1.3 Scope

This specification is intended as an extension to the existing [\[USB 2.0\]](#), [\[USB 3.2\]](#), [\[USB Type-C 2.0\]](#) and [\[USBBC 1.2\]](#) specifications. It addresses only the elements required to implement USB Power Delivery. It is targeted at power supply vendors, manufacturers of [\[USB 2.0\]](#), [\[USB 3.2\]](#), [\[USB Type-C 2.0\]](#) and [\[USBBC 1.2\]](#) Platforms, Devices and cable assemblies.

**Normative** information is provided to allow interoperability of components designed to this specification. Informative information, when provided, illustrates possible design implementation.

## 1.4 Conventions

### 1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence **Shall** be tables, figures, and then text.

In there is a conflict between a generic statement and a more specific statement, the more specific statement **Shall** apply.

### 1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

#### 1.4.2.1 Conditional Normative

**Conditional Normative** is a keyword used to indicate a feature that is mandatory when another related feature has been implemented. Designers are mandated to implement all such requirements, when the dependent features have been implemented, to ensure interoperability with other compliant Devices.

#### 1.4.2.2 Deprecated

**Deprecated** is a keyword used to indicate a feature, supported in previous releases of the specification, which is no longer supported.

#### 1.4.2.3 Discarded

**Discard**, **Discards** and **Discarded** are equivalent keywords indicating that a Packet when received **Shall** be thrown away by the PHY Layer and not passed to the Protocol Layer for processing. No **GoodCRC** Message **Shall** be sent in response to the Packet.

#### 1.4.2.4 Ignored

**Ignore**, **Ignores** and **Ignored** are equivalent keywords indicating Messages or Message fields which, when received, **Shall** result in no special action by the receiver. An **Ignored** Message **Shall** only result in returning a **GoodCRC** Message to acknowledge Message receipt. A Message with an **Ignored** field **Shall** be processed normally except for any actions relating to the **Ignored** field.

#### 1.4.2.5 Invalid

**Invalid** is a keyword when used in relation to a Packet indicates that the Packet's usage or fields fall outside of the defined specification usage. When **Invalid** is used in relation to an Explicit Contract it indicates that a previously established Explicit Contract which can no longer be maintained by the Source. When **Invalid** is used in relation to individual K-codes or K-code sequences indicates that the received Signaling falls outside of the defined specification.

#### 1.4.2.6 May

**May** is a keyword that indicates a choice with no implied preference.

#### 1.4.2.7 May Not

**May Not** is a keyword that is the inverse of **May**. Indicates a choice to not implement a given feature with no implied preference.

#### 1.4.2.8 N/A

**N/A** is a keyword that indicates that a field or value is not applicable and has no defined value and **Shall Not** be checked or used by the recipient.

#### 1.4.2.9 Optional/Optionally/Optional Normative

**Optional**, **Optionally** and **Optional Normative** are equivalent keywords that describe features not mandated by this specification. However, if an **Optional** feature is implemented, the feature **Shall** be implemented as defined by this specification.

#### 1.4.2.10 Reserved

**Reserved** is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation **May** be specified by future extensions to this specification and **Shall Not** be utilized or adapted by vendor implementation. A **Reserved** bit, byte, word, or field **Shall** be set to zero by the sender and **Shall be Ignored** by the receiver. **Reserved** field values **Shall Not** be sent by the sender and **Shall be Ignored** by the receiver.

#### 1.4.2.11 Shall/Normative

**Shall** and **Normative** are equivalent keywords indicating a mandatory requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

#### 1.4.2.12 Shall Not

**Shall Not** is a keyword that is the inverse of **Shall** indicating non-compliant operation.

#### 1.4.2.13 Should

**Should** is a keyword indicating flexibility of choice with a preferred alternative; equivalent to the phrase “it is recommended that...”.

#### 1.4.2.14 Should Not

**Should Not** is a keyword is the inverse of **Should**; equivalent to the phrase “it is recommended that implementations do not...”.

#### 1.4.2.15 Valid

**Valid** is a keyword that is the inverse of **Invalid** indicating either a Packet or Signaling that fall within the defined specification or an Explicit Contract that can be maintained by the Source.

### 1.4.3 Numbering

Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase “B” are byte values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) or are preceded by “0x” (e.g., 0xFF00) are hexadecimal values. Numbers not immediately followed by either a “b”, “B”, or “h” are decimal values.

## 1.5 Related Documents

Document references listed below are inclusive of all approved and published ECNs and Errata:

- **[USB 2.0]** – Universal Serial Bus Specification, Revision 2.0, [http://www.usb.org/developers/docs/usb20\\_docs/](http://www.usb.org/developers/docs/usb20_docs/).
- **[USB 3.2]** – Universal Serial Bus 3.2 Specification, Revision 1.0, September 22, 2017. [www.usb.org/developers/docs](http://www.usb.org/developers/docs/).
- **[USBTypeCAuthentication 1.0]**, Universal Serial Bus Type-C Authentication Specification, Revision 1.0, March 25, 2016. [www.usb.org/developers/docs](http://www.usb.org/developers/docs/).
- **[USBPDFirmwareUpdate 1.0]**, Universal Serial Bus Power Delivery Firmware Update Specification, Revision 1.0, September 15, 2016. <http://www.usb.org/developers/powerdelivery/>
- **[USBBC 1.2]** – Universal Serial Bus Battery Charging Specification, Revision 1.2 plus Errata (referred to in this document as the Battery Charging specification). [www.usb.org/developers/devclass\\_docs#approved](http://www.usb.org/developers/devclass_docs#approved).

- **[USBBridge 1.1]** – Universal Serial Bus Type-C Bridge Specification, Revision 1.1, October 10, 2017. [www.usb.org/developers/docs](http://www.usb.org/developers/docs).
- **[USBTypeCBridge 1.0]** – Universal Serial Bus Type-C Bridge Specification, Revision 1.0, March 25, 2016. [www.usb.org/developers/docs](http://www.usb.org/developers/docs).
- **[USBDP 2.0]** – Universal Serial Bus Power Delivery Specification, Revision 2, Version 1.2, March 25, 2016. [www.usb.org/developers/docs](http://www.usb.org/developers/docs).
- **[USBPDCompliance]** – USB Power Delivery Compliance Plan Version 1.0, Revision 1.1, September 2020 [http://www.usb.org/developers/docs/devclass\\_docs/](http://www.usb.org/developers/docs/devclass_docs/).
- **[USB Type-C 2.1]** – Universal Serial Bus Type-C Cable and Connector Specification, Revision 2.1, May 2021 [www.usb.org/developers/docs](http://www.usb.org/developers/docs).
- **[IEC 60958-1]** IEC 60958-1 Digital Audio Interface Part:1 General Edition 3.0 2008-09 [www.iec.ch](http://www.iec.ch)
- **[IEC 60950-1]** IEC 60950-1:2005 Information technology equipment – Safety – Part 1: General requirements: Amendment 1:2009, Amendment 2:2013
- **[IEC 62368-1]** IEC 62368-1 Audio/Video, information and communication technology equipment – Part 1: Safety requirements
- **[IEC 62368-3]** IEC 62368-1 Audio/video, information and communication technology equipment - Part 3: Safety aspects for DC power transfer through communication cables and ports
- **[IEC 63002]** IEC 63002, Interoperability specifications and communication method for external power supplies used with computing and consumer electronics devices
- **[ISO 3166]** ISO 3166 international Standard for country codes and codes for their subdivisions. [http://www.iso.org/iso/home/standards/country\\_codes.htm](http://www.iso.org/iso/home/standards/country_codes.htm).
- **[USB4]** – Universal Serial Bus 4 Specification (USB4™), Version 1.0, August 2019. [www.usb.org/developers/docs](http://www.usb.org/developers/docs).
- **[DPTC2.0]** DisplayPort™ Alt Mode on USB Type-C® Standard, Version 2.0, 12 March 2020. [www.vesa.org](http://www.vesa.org).
- **[TBT3]** see **[USB4]** Chapter 13 for Thunderbolt™ 3 device operation.