IEC 62880-1

Edition 1.0 2017-08

INTERNATIONAL STANDARD

colour inside

Semiconductor devices – Stress migration test standard – Part 1: Copper stress migration test standard

INTERNATIONAL ELECTROTECHNICAL COMMISSION

ICS 31.080.01

ISBN 978-2-8322-4732-7

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FOREWORD

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International Standard IEC 62880-1 has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/2407/FDIS	47/2416/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62880 series, published under the general title *Semiconductor devices – Stress migration test standard*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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SEMICONDUCTOR DEVICES – STRESS MIGRATION TEST STANDARD –

Part 1: Copper stress migration test standard

1 Scope

This part of IEC 62880 describes a constant temperature (isothermal) aging method for testing copper (Cu) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding (SIV). This method is to be conducted primarily at the wafer level of production during technology development, and the results are to be used for lifetime prediction and failure analysis. Under some conditions, the method can be applied to package-level testing. This method is not intended to check production lots for shipment, because of the long test time.

Dual damascene Cu metallization systems usually have liners, such as tantalum (Ta) or tantalum nitride (TaN) on the bottom and sides of trenches etched into dielectric layers. Hence, for structures in which a single via contacts a wide line below it, a void under the via can cause an open circuit at almost the same time as any percentage resistance shift that would satisfy a failure criterion.

2 Normative references

There are no normative references in this document.

NOTE Related documents are listed in the Bibliography.