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TECHNICAL REPORT



**Documentation on design automation subjects – Mathematical algorithm
hardware description languages for system level modeling and verification
(HDLMath)**

INTERNATIONAL
ELECTROTECHNICAL
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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – MATHEMATICAL ALGORITHM HARDWARE DESCRIPTION LANGUAGES FOR SYSTEM LEVEL MODELING AND VERIFICATION (HDLMath)

FOREWORD

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IEC 63051, which is a Technical Report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
91/1349/DTR	91/1396/RVC

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
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INTRODUCTION

Around the world, engineers in industries such as electronics and automobiles are developing many kinds of systems and products. However, these are developed based on conventional design processes and suffer from many design problems and long design times. Because the laws of nature can be expressed mathematically, mathematics is a good algorithmic method for the description and modeling of such systems. Mathematical modeling is also an important approach for both solving problems and visualizing the abstract concepts involved.

System LSI (Large Scale Integration) can be described at three levels of complexity as follows:

- 1) The the algorithmic level, which specifies only the algorithm used by the hardware for the problem solution;
- 2) the register transfer level, in which the registers are system elements and the data transfer between these registers is specified according to some rule;
- 3) the circuit level, where gates and flip-flops are replaced by the circuit elements such as transistors, diodes, resistors, etc.

For levels 2) and 3), VHDL (IEC 61691-1-1:2011 [1]¹) and SystemVerilog (IEC 62530:2011[2]) have already been standardized by the IEC and IEEE and have been in practical use for over twenty years.

For level 1), System C is able to describe hardware systems at the behavioral level.

The purpose of this document is to accelerate the standardization of a mathematical algorithm description language (HDLMath). HDLMath will be used to describe and verify the entire behavior of systems and/or products using mathematical algorithms of electronic systems. It is a higher level language than conventional HDL (Hardware Description Language) languages such as VHDL and SystemVerilog.

HDLMath and its design environment can support the design of many domains and applications as indicated in Table 1.

Table 1 – Examples of mathematics applications

Mathematics	Application examples
Complex numbers	Resistors, inductors, capacitors, power engineering, analysis of electric and magnetic fields, digital signal processing, image processing
Matrices and determinants	Electrical networks, computer graphics, image analysis
Laplace transforms	Circuits, power systems (generators), feedback loops
Statistics and probability	Failure rates for semiconductor devices, behavior of semiconductor materials, image analysis, data compression, digital communications techniques, error correction
Vector and trigonometry	Oscillating waves (circuits, signal processing), electric and magnetic fields, design of power generating equipment, radio frequency (RF) systems and antenna design
Differentiation and integration	Calculation of currents in a circuit, wave propagation, design of semiconductors, image analyses, design of firing circuits
Functions, polynomial, linear equations, logarithms, Euclidean geometry	Curve fitting, fuel cell design, traffic modeling, power analysis, stress analysis, determining the size and shape of parts, software design, computer graphics

¹ Numbers in square brackets refer to the Bibliography.

Recently, several HDLMath languages have already been used to design the mathematical algorithms in electronic systems. MATLAB/SIMULINK is one such popular design environment for the design and verification of various system behaviors. FinSimMath has been proposed and put to practical use by several groups to design and verify mathematical algorithms in ASIC (Application Specific Integrated Circuit) or FPGA (Field Programmable Gate Array). System C-AMS is mainly for analog circuit design and is an extension of the System C standardized by the IEEE and IEC. It is capable of describing mathematical algorithms using additional C-code extensions. IEC TR 62856:2013 [3] (BVDL, or Bird's-eye View of Design Languages) describes the features of existing design languages, as well as listing the requirements for enhancing design languages and for developing new ones.

Another purpose of this document is to add HDLMath to BVDL as a system modeling language. This document describes nine functional requirements for an HDLMath and compares current HDLMath languages from a design viewpoint. It is intended to accelerate the standardization of a mathematical algorithm design language and to establish a good system modeling environment in the world.

DOCUMENTATION ON DESIGN AUTOMATION SUBJECTS – MATHEMATICAL ALGORITHM HARDWARE DESCRIPTION LANGUAGES FOR SYSTEM LEVEL MODELING AND VERIFICATION (HDLMath)

1 Scope

A hardware description language provides a means to describe the behavior of a system precisely and concisely. This document describes the main functional requirements for an HDLMath language and compares existing HDLMath languages from the viewpoint of designers. It is intended to accelerate the standardization of a mathematical algorithm design language and to help establish a new and good system modeling and verification environment.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.