This is a preview - click here to buy the full publication

IEC®

IEC 60749-28

Edition 2.0 2021-12

PRE-RELEASE VERSION (FDIS)

Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.080.01

Warning! Make sure that you obtained this publication from an authorized distributor.

® Registered trademark of the International Electrotechnical Commission

This is a preview - click here to buy the full publication

47/2746/FDIS

FINAL DRAFT INTERNATIONAL STANDARD (FDIS)

PROJECT NUMBER:	
IEC 60749-28 ED2	
DATE OF CIRCULATION: **2021-12-17**	CLOSING DATE FOR VOTING: **2022-01-28**
SUPERSEDES DOCUMENTS: **47/2661/CDV, 47/2740/RVC**	

IEC TC 47 : SEMICONDUCTOR DEVICES			
SECRETARIAT: Korea, Republic of		SECRETARY: Mr Cheolung Cha	
OF INTEREST TO THE FOLLOWING COMMITTEES: TC 91,TC 101,TC 104		HORIZONTAL STANDARD: ☐	
FUNCTIONS CONCERNED:			
☐ EMC	☒ ENVIRONMENT	☐ QUALITY ASSURANCE	☐ SAFETY
☒ SUBMITTED FOR CENELEC PARALLEL VOTING		☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING	

Attention IEC-CENELEC parallel voting

The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Final Draft International Standard (FDIS) is submitted for parallel voting.

The CENELEC members are invited to vote through the CENELEC online voting system.

This document is a draft distributed for approval. It may not be referred to as an International Standard until published as such.

In addition to their evaluation as being acceptable for industrial, technological, commercial and user purposes, Final Draft International Standards may on occasion have to be considered in the light of their potential to become standards to which reference may be made in national regulations.

Recipients of this document are invited to submit, with their comments, notification of any relevant patent rights of which they are aware and to provide supporting documentation.

TITLE:

Semiconductor devices - Mechanical and climatic test methods - Part 28: Electrostatic discharge (ESD) sensitivity testing - Charged device model (CDM) - device level

PROPOSED STABILITY DATE: 2026

NOTE FROM TC/SC OFFICERS:

Copyright © 2021 International Electrotechnical Commission, IEC. All rights reserved. It is permitted to download this electronic file, to make a copy and to print out the content for the sole purpose of preparing National Committee positions. You may not copy or "mirror" the file or printed version of the document, or any part of it, for any other purpose without permission in writing from IEC.

This is a preview - click here to buy the full publication

CONTENTS

FOREWORD ... 6
INTRODUCTION ... 8
1 Scope ... 9
2 Normative references ... 9
3 Terms and definitions ... 9
4 Required equipment ... 10
4.1 CDM ESD tester ... 10
4.1.1 General ... 10
4.1.2 Current-sensing element ... 11
4.1.3 Ground plane ... 11
4.1.4 Field plate/field plate dielectric layer ... 11
4.1.5 Charging resistor ... 11
4.2 Waveform measurement equipment ... 12
4.2.1 General ... 12
4.2.2 Cable assemblies ... 12
4.2.3 Equipment for high-bandwidth waveform measurement ... 12
4.2.4 Equipment for 1,0 GHz waveform measurement ... 12
4.3 Verification modules (metal discs) ... 12
4.4 Capacitance meter ... 12
4.5 Ohmmeter ... 12
5 Periodic tester qualification, waveform records, and waveform verification requirements ... 13
5.1 Overview of required CDM tester evaluations ... 13
5.2 Waveform capture hardware ... 13
5.3 Waveform capture setup ... 13
5.4 Waveform capture procedure ... 13
5.5 CDM tester qualification/requalification procedure ... 14
5.5.1 CDM tester qualification/requalification procedure ... 14
5.5.2 Conditions requiring CDM tester qualification/requalification ... 14
5.5.3 1 GHz oscilloscope correlation with high bandwidth oscilloscope ... 14
5.6 CDM tester quarterly and routine waveform verification procedure ... 15
5.6.1 Quarterly waveform verification procedure ... 15
5.6.2 Routine waveform verification procedure ... 15
5.7 Waveform characteristics ... 15
5.8 Documentation ... 17
5.9 Procedure for evaluating full CDM tester charging of a device ... 17
6 CDM ESD testing requirements and procedures ... 18
6.1 Tester and device preparation ... 18
6.2 Test requirements ... 18
6.2.1 Test temperature and humidity ... 18
6.2.2 Device test ... 18
6.3 Test procedures ... 19
6.4 CDM test recording / reporting guidelines ... 19
6.4.1 CDM test recording ... 19
6.4.2 CDM Reporting Guidelines ... 19

This is a preview - click here to buy the full publication

6.5 Testing of Devices in Small Packages 19
7 CDM classification criteria 20
Annex A (normative) Verification module (metal disc) specifications and cleaning guidelines for verification modules and testers 21
A.1 Tester verification modules and field plate dielectric 21
A.2 Care of verification modules 21
Annex B (normative) Capacitance measurement of verification modules (metal discs) sitting on a tester field plate dielectric 22
Annex C (normative) Testing of small package integrated circuits and discrete semiconductors (ICDS) 23
C.1 Testing rationale 23
C.2 Procedure for Determining C_{small} 23
C.3 ICDS Technology requirements 24
Annex D (informative) CDM test hardware and metrology improvements 25
Annex E (informative) CDM tester electrical schematic 27
Annex F (informative) Sample oscilloscope setup and waveform 28
F.1 General 28
F.2 Settings for the 1 GHz bandwidth oscilloscope 28
F.3 Settings for the high-bandwidth oscilloscope 28
F.4 Setup 28
F.5 Sample waveforms from a 1 GHz oscilloscope 28
F.6 Sample waveforms from an 8 GHz oscilloscope 29
Annex G (informative) Field-induced CDM tester discharge procedures 31
G.1 General 31
G.2 Single discharge procedure 31
G.3 Dual discharge procedure 31
Annex H (informative) Waveform verification procedures 33
H.1 Factor/offset adjustment method 33
H.2 Software voltage adjustment method 36
H.3 Example parameter recording tables 38
Annex I (informative) Determining the appropriate charge delay for full charging of a large module or device 40
I.1 General 40
I.2 Procedure for charge delay determination 40
Annex J (informative) Electrostatic discharge (ESD) sensitivity testing direct contact charged device model (DC-CDM) 42
J.1 General 42
J.2 Standard test module 42
J.3 Test equipment (CDM simulator) 42
J.3.1 Test equipment design 42
J.3.2 DUT (device under test) support 43
J.3.3 Metal bar/board 43
J.3.4 Equipment setup 43
J.4 Verification of test equipment 44
J.4.1 General description of verification test equipment 44
J.4.2 Instruments for measurement 45
J.4.3 Verification of test equipment, using a current probe 45
J.5 Test procedure 47

This is a preview - click here to buy the full publication

J.5.1 Initial measurement ... 47
J.5.2 Tests ... 47
J.5.3 Intermediate and final measurement ... 47
J.6 Failure criteria ... 47
J.7 Classification criteria ... 47
J.8 Summary ... 48
Bibliography ... 49

Figure 1 – Simplified CDM tester hardware schematic ... 11
Figure 2 – CDM characteristic waveform and parameters ... 17
Figure E.1 – Simplified CDM tester electrical schematic ... 27
Figure F.1 – 1 GHz TC 500, small verification module ... 29
Figure F.2 – 1 GHz TC 500, large verification module ... 29
Figure F.3 – 8 GHz TC 500, small verification module (oscilloscope adjusts for attenuation) ... 30
Figure F.4 – GHz TC 500, large verification module (oscilloscope adjusts for attenuation) ... 30
Figure G.1 – Single discharge procedure (field charging, I_{CDM} Pulse, and slow discharge) ... 31
Figure G.2 – Dual discharge procedure (field charging, 1st I_{CDM} pulse, no field, 2nd I_{CDM} pulse) ... 32
Figure H.1 – An example of a waveform verification flow for qualification and quarterly checks using the factor/offset adjustment method ... 34
Figure H.2 – An example of a waveform verification flow for the routine checks using the factor/offset adjustment method ... 35
Figure H.3 – Example of average I_{peak} for the large verification module – high bandwidth oscilloscope ... 36
Figure H.4 – An example of a waveform verification flow for qualification and quarterly checks using the software voltage adjustment method ... 37
Figure H.5 – An example of a waveform verification flow for the routine checks using the software voltage adjustment method ... 38
Figure I.1 – An example characterization of charge delay vs. I_p ... 41
Figure J.1 – Examples of discharge circuit where the discharge is caused by closing the switch ... 43
Figure J.2 – Verification test equipment for measuring the discharge current flowing to the metal bar/board from the standard test module ... 44
Figure J.3 – Current waveform ... 44
Figure J.4 – Measurement circuit for verification method using a current probe ... 46

Table 1 – CDM waveform characteristics for a 1 GHz bandwidth oscilloscope ... 16
Table 2 – CDM waveform characteristics for a high-bandwidth (≥ 6 GHz) oscilloscope ... 16
Table 3 – CDM ESDS device classification levels ... 20
Table A.1 – Specification for CDM tester verification modules (metal discs) ... 21
Table H.1 – Example waveform parameter recording table for the factor/offset adjustment method ... 39
Table H.2 – Example waveform parameter recording table for the software voltage adjustment method ... 39

This is a preview - click here to buy the full publication

Table J.1 – Dimensions of the standard test modules 42
Table J.2 – Specified current waveform 45
Table J.3 – Range of peak current I_{p1} for test equipment 45
Table J.4 – Specification of peak current I_{p1} for the current probe verification method 46

This is a preview - click here to buy the full publication

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices, in collaboration with IEC technical committee 101: Electrostatics. It is an International Standard.

ANSI/ESDA/JEDEC JS-002-2018 has served as a basis for the elaboration of this standard. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association. ANSI/ESDA/JEDEC JS-002-2018 describes the field-induced (FI) method. An alternative, the direct contact (DC) method (not based on JS-002-2018), is described in Annex J.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

This is a preview - click here to buy the full publication

a) a new subclause and annex relating to the problems associated with CDM testing of integrated circuits and discrete semiconductors in very small packages;

b) changes to clarify cleaning of devices and testers.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/XX/FDIS	47/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

This is a preview - click here to buy the full publication

INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

This is a preview - click here to buy the full publication

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex J.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative references

There are no normative references in this document.