IEC 60749-41

Edition 1.0 2020-05

PRE-RELEASE VERSION (FDIS)

colour inside

Semiconductor devices – Mechanical and climatic test methods – Part 41: Standard reliability testing methods of non-volatile memory devices

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.080.01

47/2631/FDIS

FINAL DRAFT INTERNATIONAL STANDARD (FDIS)

PROJECT NUMBER:	
IEC 60749-41 ED1	
DATE OF CIRCULATION:	CLOSING DATE FOR VOTING:
2020-05-15	**2020-06-26**
SUPERSEDES DOCUMENTS:	
47/2584/CDV, 47/2616/RVC	

IEC TC 47 : SEMICONDUCTOR DEVICES	
SECRETARIAT: Korea, Republic of	SECRETARY: Mr Cheolung Cha
OF INTEREST TO THE FOLLOWING COMMITTEES:	HORIZONTAL STANDARD: ☐
FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY	
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TITLE:

Semiconductor devices - Mechanical and climatic test methods - Part 41: Standard reliability testing methods of non-volatile memory devices

PROPOSED STABILITY DATE: 2027

NOTE FROM TC/SC OFFICERS:

Marked and clean versions of FDIS have been attached.

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/XXXX/FDIS	47/XXXX/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The stress tests described in this part of IEC 60749 are intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention).

The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. The data retention stress can be used as a proxy to replace the high temperature storage life test when the temperature and time meet or exceed qualification requirements. Cross-temperature testing for writing and reading across the data sheet temperature range can be considered when there are demonstrated sensitivities for programming at low and reading at high temperatures or vice versa. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) can be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 41: Standard reliability testing methods of non-volatile memory devices

1 Scope

This part of IEC 60749 specifies the procedural requirements for performing valid endurance, retention and cross-temperature tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or are developed using knowledge-based methods such as in JESD94.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60749-6, *Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature*

IEC 60749-23, *Semiconductor devices – Mechanical and climatic test methods – Part 23: High temperature operating life*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology*