

This is a preview - click here to buy the full publication



JPCA

IEC PAS 62878-2-5

Edition 1.0 2015-08

PUBLICLY AVAILABLE SPECIFICATION

PRE-STANDARD



Device embedded substrate – Guidelines – Data format

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.180; 31.190

ISBN 978-2-8322-2808-1

Warning! Make sure that you obtained this publication from an authorized distributor.

CONTENTS

FOREWORD.....	4
1 Scope.....	6
1.1 Purpose.....	7
1.2 Applicable range.....	7
1.2.1 Product.....	7
1.2.2 Process.....	8
1.3 Features.....	9
1.3.1 Maintenance of the device embedded substrate structure.....	9
1.3.2 Maintenance of SiP interposer structure.....	10
1.3.3 Maintenance of design data with a virtual layer of terminal positions of embedded device(s).....	10
1.3.4 Maintenance of terminal structure and embedded device structure including SiP.....	11
1.3.5 Seamless ownership of design data.....	11
2 File description.....	12
2.1 File description summary.....	12
2.1.1 Types of data and their structure.....	12
2.1.2 File structure.....	14
2.2 3D expression.....	15
2.2.1 Coordinates.....	15
2.2.2 Position description.....	16
2.2.3 Relation between coordinate origin and board position.....	16
2.3 Layer concept.....	17
2.4 Substrate data.....	17
2.4.1 Layer map information.....	18
2.4.2 Device arrangement information.....	19
2.4.3 Basic figures.....	21
2.4.4 Net information.....	28
2.4.5 Artwork information.....	29
2.4.6 Package information.....	29
2.4.7 External port information.....	29
2.4.8 Internal port information.....	29
2.4.9 User expansion information.....	29
2.5 Defined data.....	29
2.5.1 Layer definition.....	30
2.5.2 Land definition.....	30
2.5.3 Via definition.....	31
2.5.4 Device definition.....	32
2.5.5 User expansion definition.....	33
3 Terminology.....	34
4 Commentary – Additional information.....	36
Figure 1.1 – Flow chart of design of device embedded substrate.....	7
Figure 1.2 – General concept of product.....	8
Figure 1.3 – Example of a structure of a device embedded substrate.....	10
Figure 1.4 – Examples of a structure of a SiP interposer.....	10

Figure 1.5 – Example of a laying terminal position of an embedded device in a virtual layer	11
Figure 1.6 – Example of showing structures of device embedding and terminals	11
Figure 1.7 – Example of showing structures of SiP and of a device embedding substrate	12
Figure 2.1 – Data structure	14
Figure 2.2 – One file structure (recommended)	15
Figure 2.3 – Two-File structure	15
Figure 2.4 – Definition of coordinates	16
Figure 2.5 – Position definition	16
Figure 2.6 – Relation between coordinates and board position	17
Figure 2.7 – Layer concept	17
Figure 2.8 – Construction of mounting layers	18
Figure 2.9 – Construction in the case of omission of mounting layers	19
Figure 2.10 – Layer definition in pad connection	20
Figure 2.11 – Layer definition in via connection	20
Figure 2.12 – XYZ axes rotation direction	21
Figure 2.13 – Point	22
Figure 2.14 – Area shapes	23
Figure 2.15 – Area shapes	23
Figure 2.16 – Letter data	24
Figure 2.17 – Text shape	24
Figure 2.18 – Bonding wire information	25
Figure 2.19 – Wire bonding shape	25
Figure 2.20 – Rectangular prismoid	26
Figure 2.21 – Examples of via specification	27
Figure 2.22 – Device definition	27
Figure 2.23 – Example of group such as dimension lines	28
Figure 2.24 – Data structure of net information	28
Figure 2.25 – Relation of layer definition data	30
Figure 2.26 – Land definitions	31
Figure 2.27 – Relation between hole information and land information	32
Figure 2.28 – Definitions of SiP, module and MEMS	33
Figure 2.29 – Definitions of package and mold components	33
Table 1.1 – Information required in production	9
Table 2.1 – List of data	13

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

A PAS is a technical specification not fulfilling the requirements for a standard, but made available to the public.

IEC PAS 62878-2-5 was submitted by the JPCA (Japan Electronics Packaging and Circuits Association) and has been processed by IEC technical committee 91: Electronics assembly technology.

It is based on JPCA-EB02 (2011). It is published as a double-logo IEC / JPCA PAS.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/1257/PAS	91/1264/RVD

Following publication of this PAS, which is a pre-standard publication, the technical committee or subcommittee concerned may transform it into an International Standard.

This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single period up to a maximum of 3 years, at the end of which it shall be published as another type of normative document, or shall be withdrawn.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

DEVICE EMBEDDED SUBSTRATE – GUIDELINES – DATA FORMAT

1 Scope

This part of IEC 62878 defines the data format for active and passive devices embedded inside an organic board whose electrical connections are made by means of a via, electroplating, conductive paste or printing of conductive material. The basic structures, the terminology, reliability tests and a design guide are described in the “Standard of device embedded substrate”, JPCA EB01, fourth edition.

A device embedded substrate contains device(s) in the board and is connected in a 3D way. Conventional 2D design technology using GERBER format cannot describe all the connection information in a device embedded substrate. We have several proposals to express 3D data formats but they cannot describe the structures given in EB01. The JPCA Committee for standardization of device embedded substrates has studied various formats and developed a format, FUJIKO V-1.0, which can express substrate design data in CAM data used in actual production. This Publicly Available Specification (PAS) described the FUJIKO data format.

Figure 1.1 shows the design flow of a device embedded substrate. The design data can be directly sent to a board manufacturing system using the FUJIKO format, or can be converted to CAM data and then be used in production. The data contain 3D information of coordinates and shapes of devices used. It is possible to check the status of device embedding in a board, and also make it a common knowledge in production know-how of a production line.

This PAS describes the expression of 3D data information, the concept of layers, the structure of board data, and definitions of information repeatedly used in design.