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10861**

**ANSI/IEEE
Std 1296**

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**Information technology—
Microprocessor systems—
High-performance synchronous 32-bit bus:
MULTIBUS II**

*Technologies de l'information –
Systèmes à microprocesseurs –
Bus 32 bits synchrone à haute performance:
MULTIBUS II*



Reference number
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Abstract: The operation, functions, and attributes of a parallel system bus (PSB), called MULTIBUS II, are defined. A high-performance backplane bus intended for use in multiple processor systems, the PSB incorporates synchronous, 32-bit multiplexed address/data, with error detection, and uses a 10 MHz bus clock. This design is intended to provide reliable state-of-the-art operation and to allow the implementation of cost-effective, high-performance VLSI for the bus interface. Memory, I/O, message, and geographic address spaces are defined. Error detection and retry are provided for messages. The message-passing design allows a VLSI implementation, so that virtually all modules on the bus will utilize the bus at its highest performance—32 to 40 Mbyte/s. An overview of PSB, signal descriptions, the PSB protocol, electrical characteristics, and mechanical specifications are covered.

Keywords: high-performance synchronous 32-bit bus, MULTIBUS II, system bus architectures

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Information technology— Microprocessor systems— High-performance synchronous 32-bit bus: MULTIBUS II

Sponsor

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of the
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In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote.

In 1990, ANSI/IEEE Std 1296-1987 was adopted by ISO/IEC JTC 1, as draft International Standard ISO/IEC/DIS 10861. This draft was subsequently approved by ISO/IEC JTC 1 in the form of this edition, which is published as International Standard ISO/IEC 10861 : 1994.



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Introduction

(This introduction is not a normative part of ISO/IEC 10861 : 1994 [ANSI/IEEE Std 1296, 1994 Edition], but is included for information only.)

In the last decade, the avalanche of new microcomputer technology, especially VLSI, threatened to obsolete products almost before they went into production. To buffer users from this onrush of technology, Intel helped develop standard interfaces. One of the most notable was the MULTIBUS I system bus, which was used as the basis for a standard by the IEEE in 1983 as IEEE Std 796-1983 (after going through a 5-year review and revision process).

In the early 1980s, Intel recognized that the trends toward multiprocessing and more sophisticated microcomputer-based systems called for an advanced 32-bit system bus architecture. Intel called this new bus MULTIBUS II. In continuing to pioneer the open systems technology, which included multiprocessing, four critical requirements were observed: technical credibility, processor independence, standardization, and openness to all levels of integration. Early in the development of the new bus, Intel established a "MULTIBUS II Development Consortium." The consortium gave the new bus a technical credibility that few buses, especially those defined only among board vendors, can match. The companies in the consortium also represented all microprocessor families; included in the group were 68020, 32032, 80386, and Z8000 board and system users, thus ensuring that the bus is easily adaptable to virtually any manufacturer's processor.

The primary benefits being sought in the creation of this new bus were high-performance multiprocessing, high system reliability, ease-of-use by system designers, and improved cost/performance.

Specific bus features were developed in response to these objectives. The 32 Mbyte/s message passing of the bus provides a bus that acts like a very high-speed network connection for multiple processors (or processor equivalents). There is a recognition that the bus is no longer to interconnect a CPU with its memory and I/O; instead the bus is to interconnect whole stand-alone processors with each other and with intelligent "sub-systems-on-a-board."

System reliability is enhanced by the features of bus parity, synchronous operation, negative acknowledge, transfer retries, geographic addressing, and advanced backplane design. Ease-of-use by system designers is implemented primarily through the geographic addressing, which provides for dynamic system configuration. The bus encourages the use of software programmable configuration options (and discourages any use of mechanical jumpers). The standardization of the high-level message-passing protocol also gives the system designer an easy-to-use capability for interprocessor communication.

The cost/performance objective of the bus is delivered through its specification of a realizable 32 to 40 Mbyte/s bus bandwidth. Virtually all boards designed to the bus can achieve this bus utilization factor due to the high-level protocol called out in the specification, and thus the availability of standard, high-performance and cost-effective VLSI components to actually implement this level of performance. For example, this specification and the VLSI make it possible for eight concurrent 4 megabyte/second transfers to take place on the bus. This, or other combinations of transfers that add up to 32 Mbyte/s, demonstrate the real cost/performance advantages of the bus for multiprocessor applications.

In 1983 MULTIBUS II was introduced to the IEEE standards process as a part of the considerations for the P896 (Future Bus) working group activities. In the 1984/1985 time frame the MSC (Microcomputer Standards Committee, of the TCMM) formed an independent study group for MULTIBUS II. During this time the many active participants of the group proceeded to thoroughly review and make changes to the proposed draft. In early 1986 the group was assigned a formal project number P1296. During the remainder of 1986, the draft was passed by the Working Group and the MSC after thorough review, discussion, and changes. In 1987, the draft was presented for Sponsor ballot and, after passing, presented to the June 1987 meeting of the IEEE Standards Board.

The IEEE Standards Board calls attention to the fact that there are patents claimed and/or pending on many aspects of this bus by Intel Corporation. IEEE takes no position with respect to patent validity. Intel Corporation has assured the IEEE that it is willing to grant a license for these patents on reasonable and nondiscriminatory terms to anyone wishing to obtain such a license. The general terms of the license are a one-time administration fee of \$100 for a nonexclusive perpetual license. Intel Corporation's undertakings in this respect are on file obtained from the legal department of Intel Corporation whose address is Intel Corporation, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124.

There were many contributors to the standards review process, but the following members deserve special mention for their active participation:

Task Force Coordinators: Jack Blevins
Maurice Hubert
Hubert Kirrmann
Jim Nebus
Secretary of Working Group: Steve Cooper
Original Study Group Chairman: Paul Borrill
Original Draft Editor: Scott Tetrick

The P1296 Working Group that prepared this standard had the following membership:

Richard W. Boberg, *Chair*

Web Augustine	Gene Freehauf	Ken Smith
Jack Blevins	Maurice Hubert	Michael Thompson
Paul Borrill	Hubert Kirrmann	Scott Tetrick
Steve Cooper	Klaus Mueller	Eike Waltz
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	Don Nickel	

The following members of the Technical Committee on Microprocessors and Microcomputers were on the balloting body:

Andrew Allison	Martin Freeman	Deene Ogden
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J. Robert Davis	Tom Leonard	Carl Warren
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IEEE Std 1296-1987 was approved by the American National Standards Institute on February 8, 1987 and was reaffirmed by IEEE on March 17, 1994.

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Information technology—Microprocessor systems—High-performance synchronous 32-bit Bus: MULTIBUS II

1. General overview

1.1 Scope

This International Standard defines the operation, functions, and attributes of the IEEE 1296 bus standard.

- a) This standard defines a high-performance 32-bit synchronous bus standard.
- b) The bus standard must have a design-in lifetime of 10 years with backward compatibility.
- c) The standard is intended for general purpose applications to optimize block transfers, including protocol for message passing. For real-time applications, the bus will provide a means of ensuring an upper limit to message delivery time.
- d) The standard is intended to be compatible with existing IEC mechanical standards (IEC Pub 297-1,¹ 297-3, and 603-2) with recognition of the need for special front panels to address ESD, EMI, and RFI requirements.
- e) Options within the standard will be clearly identified.
- f) The standard is intended to support multiple processor modules in a functionally partitioned configuration and heterogeneous processor types in the same system.
- g) The standard is intended to support heterogeneous processor types in the same system.
- h) Message-passing format and protocol is intended for future migration to a serial system bus.

1.2 Normative references

The following standards contain provisions which, through references in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

DIN 41612, Two Part Connectors for Printed Board, GRIB, to 54 mm, Common Mounting Features, Survey of Types.²

¹Information on references can be found in 1.2.

²DIN publications are available from the Deutsches Institut für Normung, Burggrafenstrasse 6, D-1000 Berlin 30, Germany.

IEC 297-1 : 1986, Dimensions of mechanical structures of the 482,6 mm (19 in) series—Part 1: Panels and racks.³

IEC 297-3 : 1984, Dimensions of mechanical structures of the 482,6 mm (19 in) series—Part 3: Subracks and associated plug-in units.

IEC 603-2 : 1988, Connectors for frequencies below 3 MHz for use with printed boards—Part 2: Two-part connectors for printed boards, for basic grid of 2,54 mm (0,1 in), with common mounting features.

IEEE Std 1101-1987, IEEE Standard for Mechanical Core Specifications for Microcomputers (ANSI).⁴

³IEC standards are available from the IEC Sales Department, Case Postale 131, 3 rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse.

⁴IEEE publications are available from the Institute of Electrical and Electronics Engineers, Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.